CDB49400

Evaluation Board for CS49400 Family DSP

Features

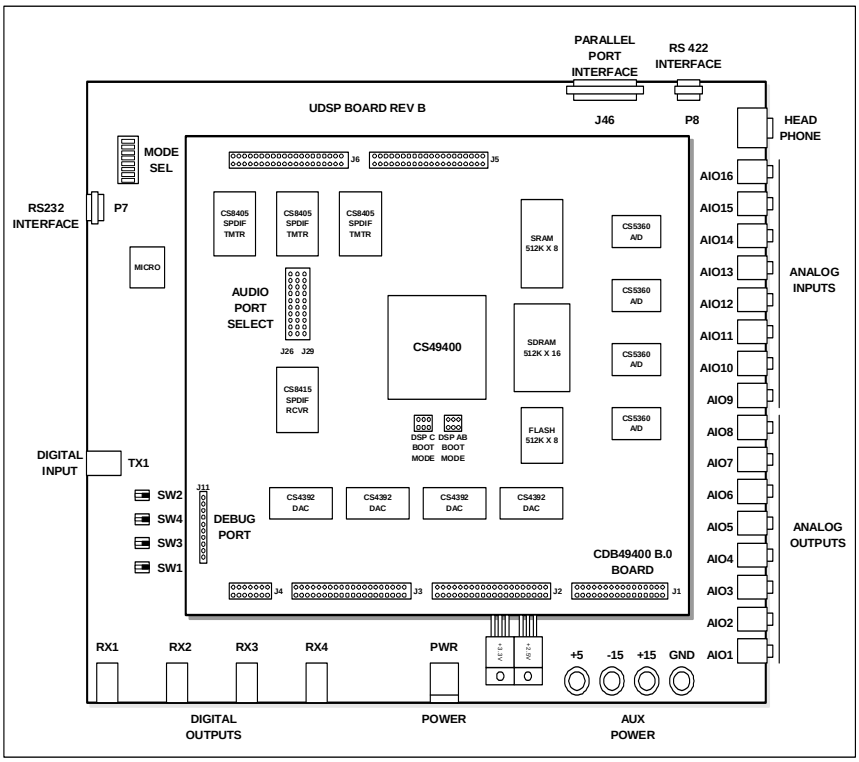
- 8 Discrete analog inputs using CS5360 ADCs
- 8 Discrete analog outputs using CS4392 DACs
- Supports 16 Channel decoding capability of the CS49400
- 1Digital input using the CS8415A S/PDIF receiver
- 3 Digital outputs using the CS8405 S/PDIF transmitter
- On board memories for special post processing needs
- On board debug functionality for DSPC

Description

The CDB49400 is an evaluation board for the CS49400 (**144 Pin**) family of DSPs. It allows customers to develop, download and test custom algorithms on the CS49400. The onboard PLD on the UDSP can route data to any of the audio data inputs and supply clocks in many different combinations to the CS49400. The board interfaces to a PC via a ECP parallel port. Optical and RCA connectors are used to interface with DVD players, powered speakers and other test equipment. Compressed data can be delivered in IEC61937 format via the S/PDIF port. PCM data can be accepted through the digital input connector or from the on-board ADCs. Together these boards supports all the decoding algorithms developed by Cirrus Logic.

ORDERING INFORMATION

CDB49400 Evaluation Board



Preliminary Product Information

This document contains information for a new product.
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1. QUICK START

A PC with an ECP parallel port, an optical S/PDIF data source, and powered speakers are required to use the CDB49400.

1) Install the drivers supplied with the board on the PC. Refer to "INSTALLATION OF BOARD CONTROL SOFTWARE" on page 24 for details on installing the drivers.
2) Connect the supplied parallel port cable to J46 and to the computer's parallel port.
3) Connect the optical output from a DVD player to RXI.
4) Connect a powered speaker to AIO1 [The output channels are mapped as follows: AIO1 - Left, AIO2 - Center, AIO3 - Right, AIO4 - Left Surround, AIO5 - Right Surround, AIO6 - Surround Back Left, AIO7 - Surround Back Right, AIO8 - Subwoofer]. More speakers can be connected to the line level outputs as required by each application.
5) Connect the supplied power supply to the power connector on the board.
6) Verify that LEDs D1, D7, D9, D11 on the UDSP board and D9, D13, D17, D20 on CDB49400 daughter card are lit. LED D2 will flash to indicate that the PLD on the UDSP is functional.
7) Open a DOS window and navigate to the C:\CS49400\CDB49400\Configs directory.
8) Type in "setpld -r 99" on the DOS prompt. (This reads the PLD version register and verifies that the PC can communicate with the board). If the driver generates the error message "!!! Board does not appear to be connected !!!", then your parallel port address may not be 0x378 or your port is not ECP capable. If your parallel port address is not 0x378, depress the reset switch S3 and type in "setpld -r 99 -p3bc" or "setpld -r 99 -p278" to communicate using a different parallel port address.
9) Verify that the value returned is not 0, 99 or 0xff, and LED D1 has turned OFF.
10) If the above steps give an error, check all the jumpers and switches as described in "DEFAULT JUMPER SETTINGS ON THE CDB49400" on page 11 and repeat the above procedure. Refer to "BOARD CONTROL SOFTWARE" on page 21 and verify that the drivers and PC have been set up as described.
11) If the above steps give the expected results, type in "PCM_49400", "PCM_49400 -p3bc", or "PCM_49400 -p278" (depending on your parallel port address) at the DOS prompt, This batch file will configure the PLD, boot the DSP, and configure all the peripherals.
12) If the batch file loads successfully, the GPIO20 LED will flash. This indicates that the DSP is running the downloaded code.
13) Play a CD to send PCM data to the DSP via the RX1 optical connector, GPIO21 will turn on and audio will be heard on the output.

The batch file use various files to configure the software, board, and the DSP code. Each text file has been commented. A sample batch file has been included in "PCM_49400.BAT" on page 15 for reference. Various batch files for the commonly used applications have been supplied with the software. These batch files can be run from the DOS prompt like the "PCM_49400.BAT" file. Use caution while editing and making changes to these files. DO NOT move any jumpers or switches unless it is required for additional testing, or instructed to do so by a Cirrus Logic FAE.

2. HARDWARE OVERVIEW

The CDB49400 board is designed to allow the user to fully evaluate the CS49400 user programmable audio DSP. As seen in block diagram on page 1, the CDB49400 board consists of daughter card plugged into a mother board. The mother board referred to as the UDSP has a microcontroller, Programmable Logic Device (PLD), power conditioning, input/output connectors, jumpers, switches and many other circuits as seen in "UDSP SCHEMATICS" on page 43. The microcontroller enables the board to run in stand alone mode and control all the devices on the mother board as well as daughter card. The PLD has number of multiplexers which enable the data/clocks and control logic to be routed to the DSP in a number of combinations. The PLD is controlled by the microcontroller if SW1 is in the OFF position or by the parallel port if SW1 is in the ON (default) position. Input/output connectors enable digital or analog data to be sent to/from the daughter card. Switches enable the microcontroller to perform various operations in standalone mode. Currently the standalone features of the board are not supported and a PC must be used to communicate with the board. The UDSP has many devices and connectors that are not used for the CDB49400 board.

The daughter card that plugs into the UDSP has a CS49400 DSP, four CS5360 ADCs, one CS8415A S/PDIF Receiver, three CS8405A S/PDIF Transmitters, four CS4392 DACs, SRAM, SDRAM and Flash as seen in "CDB49400 SCHEMATICS" on page 26.

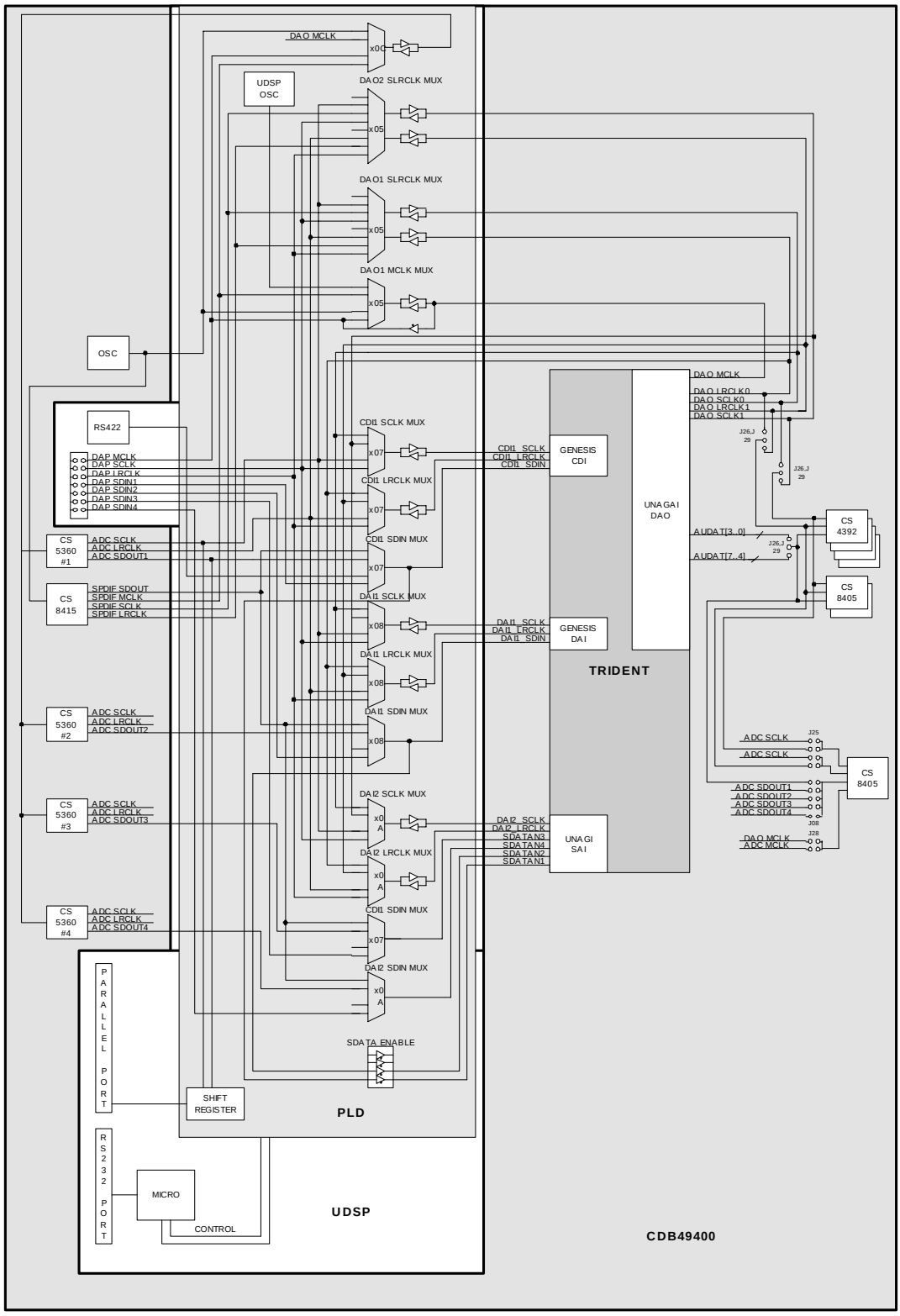
The CS49400 has 3 cores in it. The decoder core is referred to as DSPAB and the postprocessor is referred to as DSPC. Both DSPs can be booted from a PC via a parallel port. They can be configured to communicate via SPI or I^2C®, serial interfaces or Motorola® or Intel® parallel interfaces. However all the other devices on the board are configured in SPI mode as this is the default configuration of the CDB49400. As seen in "Audio Data/Clock Routing" on page 6, the Compressed Data Input (CDI), Digital Audio Input (DAI) and Serial Audio Input (SAI) inputs of the DSP are connected to the PLD. The output of the ADC, and S/PDIF receiver are connected to the PLD. The PLD on the UDSP can be configured to route clocks, data from the ADC, S/PDIF receiver to any input port on the DSP. Configuration files for the PLD are supplied for common clocking and data delivery schemes. Custom configuration files for data delivery are available on request. Four DAC and three S/PDIF transmitters are connected to the Digital Audio Output (DAO) ports of the DSP. Data sent to these output devices are selected by jumpers J26 and J29.

Three types of memory are available. On the CDB49400 SDRAM and SRAM are available for use by applications with any special processing needs. FLASH is available to store application code and boot the DSP in a Host Controlled Boot operation. Details of the External memory interface will be discussed in "External Memory Interface" on page 10.

LEDs are connected to GPIO20 and GPIO21 and used to indicate the status of application code on the DSP. Other LEDs indicate power.

All signals entering or leaving the DSP are accessible via headers. A debug port accessible to a PC via the parallel port, is used to develop and debug code on DSPC.

The CDB49400 board is powered off +15V, -15V and 5V DC supplies. These are regulated and filtered to meet the various voltage requirements of the individual circuits. The power supply supplied with the system, connected to J35 can be used to power the board. Additionally power can be supplied to the board via the binding posts to aid in debug, or isolation of noise generation.



Note:
1. DAO_MCLK is the Master CLK for the system execpt the ADC
2. AUDAT3 and AUDAT7, are routed to XMT connector
3. Change PLD code for new routing.

Figure 1. Audio Data/Clock Routing

3. SOFTWARE OVERVIEW

A suite of software has been provided with CDB49400. Currently the CDB49400 is controlled by the software described in "BOARD CONTROL SOFTWARE" on page 21. Figure 2 describes the typical structure of a batch file that used to setup the board and boot the DSP. This flow chart describes the flow of the "PCM_49400.BAT" on page 15.

All batch files first call "SET_INI.BAT" which gets an environment variable to the location of "CDB49400.INI" file described on page 19. This INI file contains the board configuration of all the devices on the CDB49400 to the software drivers. The "SET_INI.BAT" batch file must be executed every time a new DOS session is started. Next the file "RESET.BAT" on page 20 is called. This batch file mutes the DACs and resets all the devices including the DSP on the CDB49400 board. Next the "SPDIF_ANA_IN_DIG_ANA_OUT.BAT" file described on page 17 is called to boot and configure each device (except the DSP) in the modes described in the batch file. The PLD is also configured as shown in Figure 3, "Sample Data/Clock Routing," on page 9. At this time all peripherals are setup and ready to accept data. The DSP is then booted using the "u40ld" command. This command follows the "Host Boot Procedure" described in the CS49400 datasheet. Once code has been downloaded to both DSPAB and DSPC, DSPC is configured and kickstarted first. Next DSPAB is configured and kickstarted.

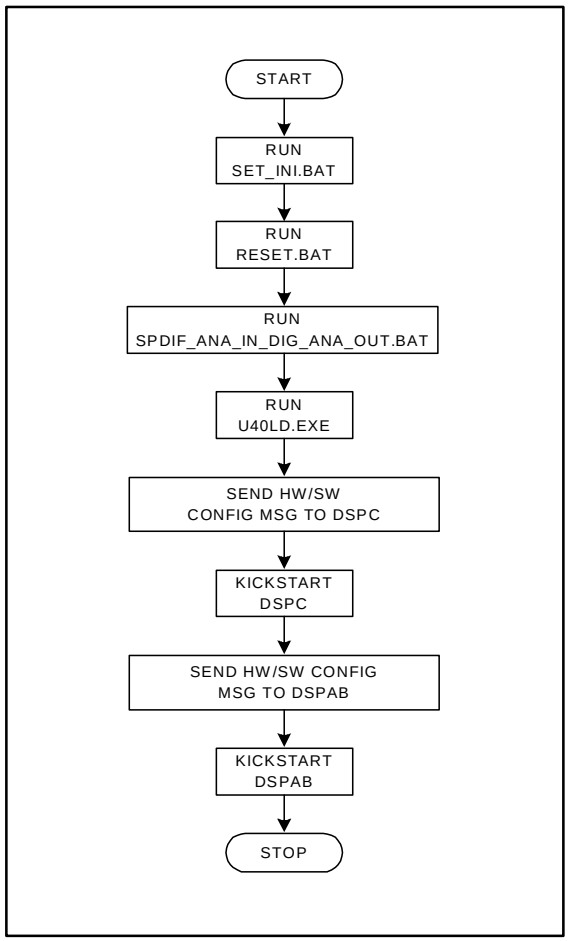


Figure 2. Software Overview

4. AUDIO DATA AND CLOCK ROUTING

The audio data and clocks are routed via the PLD. The PLD configuration file has been included in "SPDIF_ANA_IN_DIG_ANA_OUT.BAT" on page 17 describes how the PLD is set up. Depending on the application, the appropriate board config batch file needs be called from the main batch file. The following commonly used batch file is included with the kit. Please contact your FAE for additional batch files if necessary.

4.1 SPDIF_ANA_IN_DIG_ANA_OUT.BAT

This batch file configures the board to accept digital data from the RX1 (optical connector) and analog data on AIO11 and AIO12 (RCA connectors). The clock and data routing is shown in Figure 3, "Sample Data/Clock Routing," on page 9. Few of the signals are routed via the UDSP PLD. The S/PDIF receiver accepts digital data from RX1 and recovers MCLK for the system. If a stream is not present, the S/PDIF receiver switches to the local 12.288 Mhz oscillator. The ADC is set to master SCLK and LRCLK for the input ports. Data from the ADC is routed to the DAI port. The S/PDIF receiver slaves to SCLK and LRCLK generated by the ADC, and sends data to the CDI port of the DSP. MCLK is also routed to the DSP. The DSP slaves to MCLK from the S/PDIF receiver, and masters SCLK and LRCLK for the output ports. Data routed to the DACs and S/PDIF transmitters is selected by jumpers J26 and J29. The digital data is output on RX1, RX2, RX3 and RX4 (optical connector). For RX4 to transmit data, DSP must be configured to be a S/PDIF transmitter. Analog data is output on AIO1 to AIO8 (RCA connectors) with the following mapping:

- AIO1-Left
- AIO2 - Center
- AIO3 - Right
- AIO4 - Left Surround
- AIO5 - Right Surround
- AIO6 - Left Surround Back
- AIO7 - Right Surround Back
- AIO8 - Sub woofer

The batch file configures the S/PDIF receiver, DACs and the S/PDIF transmitter for I2S data format. Please refer to the CS8415A, CS4392 and CS8405A data sheets for more info on configuring these devices.

The batch file use, the drivers documented in "BOARD CONTROL SOFTWARE" on page 21.

5. BOOT MODES AND DEBUG PORT

The CS49400 has 4 possible boot modes, which are selected by appropriately strapping the FHS[2..0] and UHS[2..0] mode select pins. Jumper settings for the various boot modes are documented in Table 1 on page 11 and Table 2 on page 11. Both DSPAB and DSPC must have the same host interface mode.

Currently the board is configured for SPI host boot and SPI control on both DSPAB and DSPC. Please contact the factory if additional boot or control modes are required. Other audio devices such as the CS8415A, CS8405A and the CS4392 are configured for SPI control and their SPI device addresses are set in the CDB49400.ini file.

Please see the CS49400 data sheet for further information on the various supported boot and control modes.

5.1 Debug Port for DSPC

The command line debugger for DSPC is called CID and uses the parallel port interface on the CDB49400. CID is included as part of the software development kit CD-ROM. Please refer to the documentation in the Software User manual for details on how to use CID.

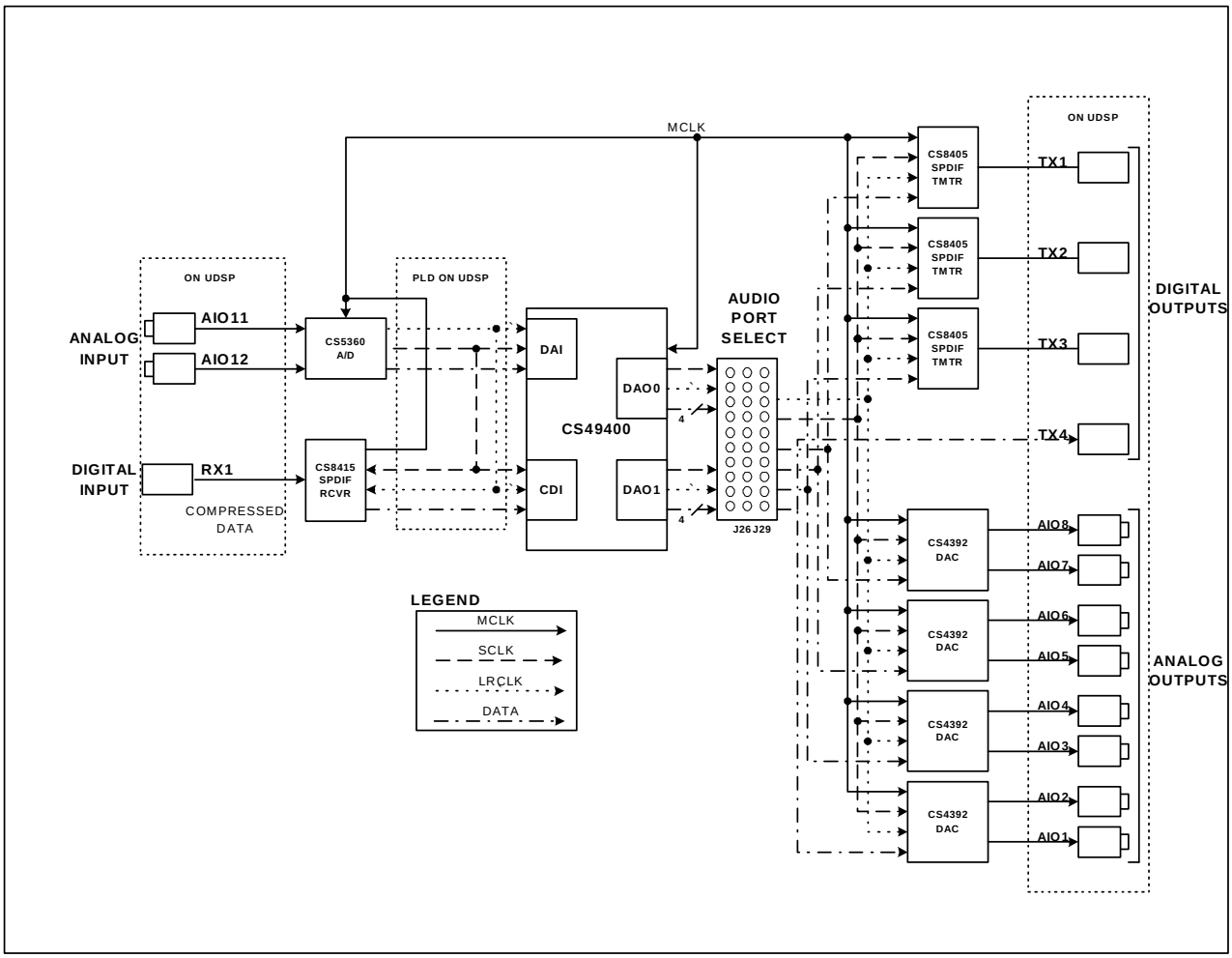


Figure 3. Sample Data/Clock Routing

6. EXTERNAL MEMORY INTERFACE

The CDB49400 supports all 3 types of memory that can be interfaced to CS49400, SRAM, SDRAM and FLASH. SDRAM and SRAM can be used for additional X-data memory on DSPC. Use of external SDRAM or SRAM is application dependent. Please refer to the relevant application code documentation to determine if external memory is required. FLASH is used to store application code images for both DSPAB and DSPC. The following sections describe these memory types in more detail.

6.1 SDRAM (U8)

The CDB49400 board includes a 16-MBIT (1M X 16 bit) of 100 MHz SDRAM connected to the glueless SDRAM interface of the CS49400. SDRAM is memory mapped into the internal X memory space and runs at DSP core speed. The SDRAM interface shares the same address and data pins as the SRAM and FLASH interface but has separate control pins. Although the CS49400 can support using all 3 memories in a given design, a typical application would include SDRAM and FLASH or SRAM and FLASH.

6.2 SRAM (U5)

The CDB49400 board includes 4 MBits (512K X 8) of SRAM connected to the external memory interface of the CS49400. Like SDRAM, SRAM is memory mapped into the external X-memory space. Please see the CS49400 data sheet for detailed SRAM timing information. Both FLASH and SRAM use the same external memory interface on the CS49400. The CDB49400 uses address bit 19 of the CS49400 external address bus to map FLASH into the lower half of the external memory space and SRAM into the upper half of the external memory space.

6.3 FLASH (U9)

The CDB49400 board includes 4 Mbits (512K X 8) of byte-wide FLASH EPROM connected to the external memory interface of the CS49400. FLASH is used to store application code images for DSPAB and DSPC. DSPC also supports in-circuit FLASH programming. Please contact your FAE for more information on FLASH programming details.

7. DEFAULT JUMPER SETTINGS ON THE CDB49400

The following tables list the default settings of all the jumpers and switches. Do not move any switches or jumpers unless required for a specific application.

7.1 Host Interface / Boot Modes

FHS2 J34	FHS1 J27	FHS0 J17	Host Interface/Boot Mode
1	0	0	Serial I^2C® /Via DSPC
1	0	1	Serial SPI /Via DSPC
1	1	0	8-bit Intel® /Via DSPC
1	1	1	8-bit Motorola® /Via DSPC

Table 1: DSPAB Boot Modes/ Host Interface

UHS2 J15	UHS1 J16	UHS0 J20	Host Interface/Boot Mode
1	0	0	Serial I^2C® /Via External Host
1	0	1	Serial SPI /Via External Host
1	1	0	8-bit Intel® /Via External Host
1	1	1	8-bit Motorola® /Via External Host

Table 2: DSPC Boot Modes/ Host Interface

7.2 Host Interface / Boot Mode Jumpers

Jumper	Purpose	Position	Function
J20	Boot mode select - UHS0	1-2* 2-3	High Low
J16	Boot mode select - UHS1	1-2 2-3*	High Low
J15	Boot mode select - UHS2	1-2* 2-3	High Low
J17	Boot mode select - FHS0	1-2* 2-3	High Low
J27	Boot mode select - FHS1	1-2 2-3*	High Low
J34	Boot mode select - FHS2	1-2* 2-3	High Low

Table 3: Boot Mode Jumpers

7.3 Debug Port Interface Jumpers

Jumper	Purpose	Position	Function
J10	Select Debug Port Clock interface for DSPC.	1-2 2-3*	Debug using Debug Dongle on J11 Debug using Parallel Port on UDSP
J12	Select Debug Port Data interface for DSPC.	1-2 2-3*	Debug using Debug Dongle on J11 Debug using Parallel Port on UDSP

Table 4: Debug Port Interface Jumpers

7.4 Communication

Jumper	Purpose	Position	Function
J35	Connects the Rx SDA/CDOUT pin to either the $I^2C^®$ or SPI bus.	1-2* 2-3	SDA/CDOUT = SPI MISO bus SDA/CDOUT = $I^2C^®$ SDA bus
J36	Connects the Rx AD1/CDIN pin to the SPI bus	1-2* 2-3	ADI/CDIN =SPI MOSI bus ADI/CDIN = LO
J38	Select the AD0 Address Bit for $I^2C^®$ mode (CS8415A)	1-2* 2-3	ADO = HI ADO = LO
J47	Select the AD0 Address Bit for $I^2C^®$ mode (CS8405)	1-2* 2-3	ADO = HI ADO = LO

Table 5: CS8415A S/PDIF Receiver and CS8405 S/PDIF Transmitter Communications

Jumper	Purpose	Position	Function
J9	Select the AD0 Address Bit for $I^2C^®$ mode (CS4392)	1-2* 2-3	ADO = HI ADO = LO

Table 6: CS4392 DAC Communications

7.5 Serial Audio

Jumper	Purpose	Position	Function
J25	Selects LRCLK/SCLK source for CS8405 (U44)	1-2* 3-4 5-6* 7-8	LRCLK = DSP LRCLK (see J26,J29) LRCLK = ADC LRCLK SCLK = DSP LRCLK (see J26,J29) SCLK = ADC SCLK
J28	Selects MCLK source for CS8405 (U44)	1-2* 3-4	MCLK = DSP MCLK LRCLK = ADC MCLK
J8	Selects Data source for CS8405 (U44)	1-2* 3-4 5-6 7-8 9-10	SDIN = DSP DAO C (see J26,J29) SDIN = ADC SDOUT1 SDIN = ADC SDOUT2 SDIN = ADC SDOUT3 SDIN = ADC SDOUT4

Table 7: CS8405 Clocks/ Data Input

7.6 Other Settings

Jumper	Purpose	Position	Function
J30	Select CLKIN/XTAL1 input to the DSP	1-2* 2-3	External 12.288 OSC to CLKIN 12.288 XTAL to XTAL1 Note: J33 must be installed if XTAL1 is used
J33	Connect XTAL0 to an external oscillator	1-2	12.288 XTAL to XTAL0 Note: J30, 2-3 must be installed if XTAL0 is used
J31	Select clock source for DSP	1-2 2-3*	DSP uses external 12.288 MHz clock DSP uses internal PLL
J24	Select 3.3V / 2.5V power supply for DSP I/O	1-2* 2-3	3.3V for DSP I/O 2.5V for DSP I/O
J32	Measure core current	1-2*	Use DMM to measure current
J7	Set the ADC to Master/Slave SCLK and LRCLK	1-2 2-3*	ADC slaves to SCLK and LRCLK ADC masters SCLK and LRCLK
J26,J29	Select the Data/Clock source to the CS4392 and CS8405	J29-2,J26-4* J26-3,J26-4 J29-3,J26-6* J26-5,J26-6 J29-4,J26-8* J26-7,J26-8 J29-5,J26-10* J26-9,J26-10 J29-6,J26-12* J26-11,J26-12 J29-7,J26-14* J26-13,J26-14	DAO_SCLK0 to DAO_SCLK DAO_SCLK1 to DAO_SCLK DAO_LRCLK0 to DAO_LRCLK DAO_LRCLK1 to DAO_LRCLK DAO_AUDAT0 to DAO_AUDATA DAO_AUDAT4 to DAO_AUDATA DAO_AUDAT1 to DAO_AUDATB DAO_AUDAT5 to DAO_AUDATB DAO_AUDAT2 to DAO_AUDATC DAO_AUDAT6 to DAO_AUDATC DAO_AUDAT3 to DAO_AUDATD DAO_AUDAT7 to DAO_AUDATD

Table 8: Miscellaneous Jumpers

Note: " * " - Indicates default position.

8. DEFAULT JUMPER SETTINGS ON UDSP

The UDSP board has many jumpers and switches. All jumpers and switches applicable the CDB49400 daughter card are listed in the table below. Do not move any switches or jumpers unless required for a specific application.

Jumper	Purpose	Position	Function
JP1	Enable/Disable clock for the PLD	1-2* 2-3	Enable Clock for PLD Disable Clock for PLD
J40	Select voltage level for chip selects	1-9 9-17* 2-10 10-18* 3-11 11-19* 4-12 12-20* 5-13 13-21* 6-14 14-22* 7-15 15-23* 8-16 16-24*	CS0 pulled up to 3.3 V CS0 pulled up to 2.5 V CS1 pulled up to 3.3 V CS1 pulled up to 2.5 V CS2 pulled up to 3.3 V CS2 pulled up to 2.5 V CS3 pulled up to 3.3 V CS3 pulled up to 2.5 V CS4 pulled up to 3.3 V CS4 pulled up to 2.5 V CS5 pulled up to 3.3 V CS5 pulled up to 2.5 V CS6 pulled up to 3.3 V CS6 pulled up to 2.5 V CS7 pulled up to 3.3 V CS7 pulled up to 2.5 V
J44	Select communication mode for daughter card	1-2 2-3*	Daughter card set for I^2C® mode Daughter card set for SPI mode
JP2	Set the micro in Run/Program mode	1-2* 2-3	Set the micro in Run mode Set the micro in Program mode
SW1	Select control mode for DSP	ON* OFF	CDB49400 controlled by Parallel port CDB49400 controlled by RS232 port Note: The RS232 control is not yet supported
SW2	Select which debug port is accessed by the parallel port	ON* OFF	DSPC debug port accessed by parallel port. Reserved

Table 9: Miscellaneous Jumper/Switch Default Settings for UDSP

Note: " * " - Indicates default position.

APPENDIX A: PCM_49400.BAT

```
REM Version: $Name:  $
@echo off
echo INPUT: RX1 to CDI
echo ANA.OUTPUTS:(AIO1=L,AIO2=C,AIO3=R,AIO4=Ls,AIO5=Rs,AIO6=Sbl,AIO7=Sbr,AIO8=SUB)
echo DIG.OUTPUTS:(TX1=L C, TX2=R Ls, TX3=Rs Sbl)
REM Set Environment variable for command line drivers
@call set_ini.bat
REM Reset all devices, DSP and initialize debugger; Mute DACs
@call board\reset.bat %1 %2
REM Configure board for SPDIF IN, Digital/analog out
@call board\spdif_ana_in_dig_ana_out.bat %1 %2
REM Load these images to DSPAB and DSPC
u40ld ..\..\release\uld\cos_6dot1_ab_494xx1_04.uld ..\..\release\uld\spp_c_494xx1_01.uld %1
REM Configure DSPC
REM Slave MCLK master SCLK/LRCLK
ucmd -f..\..\hw\output_a1_c.cfg -ddspc %1
REM Set clock dividers for SCLK=MCLK/4 and LRCLK=SCLK/64
ucmd -f..\..\hw\mclkb4sclkb64_c.cfg -ddspc %1
REM Remap channels (AIO1=L, AIO2=C, AIO3=R, AIO4=Ls, AIO5=Rs, AIO6=Sbl, AIO7=Sbr, AIO8=SUB)
ucmd -f..\..\hw\mode011_c.cfg -ddspc %1
REM Kickstart for DSPC
ucmd -f..\..\sw\ks_c.cfg -ddspc %1
REM DSPC Configured and running
REM Configure DSPAB
REM Set CDI port for PCM
ucmd -f..\..\hw\inputa2.cfg -ddspab %1
REM Enable PCM Decoding
ucmd -f..\..\sw\pcm_ab.cfg -ddspab %1
REM Set PLL for 75 MHz
ucmd -f..\..\hw\pll75_ab.cfg -ddspab %1
REM Kickstart DSPAB with the PLL Enabled
ucmd -f..\..\sw\ks_pll_ab.cfg -ddspab %1
REM DSPAB Configured and running
```

```
REM Unmute the DACs
setpld -w 02 00 %1
@echo on
```

APPENDIX B: SPDIF_ANA_IN_DIG_ANA_OUT.BAT

```
@ ECHO OFF
REM Version: $Name:  $
echo Configuring Peripherals.....
REM Set up the Board for Compressed/Analog In Analog/Digital Out
REM Inputs:CDI RX1
REM Inputs: DAI AIO11 & AIO12
REM Outputs (ANALOG): AIO [1..8]
REM Outputs (DIGITAL): TX [1..4]
REM Data format to/from DSP: I2S 24 Bit
REM Clocks:SDIF RCVR generates MCLK.
REM ADC masters SCLK and LRCLK for the SPDIF RCVR, DAI and CDI port
REMDSP Slaves to MCLK and masters SCLK and LRCLK on DAO
REM Set the clock source for ADC to SPDIF from DC and set MCLK as an output
setpld -w 0c 09 %1 %2
REM set the 8415 in slave mode and the output format to to I2S -16 bit
ucmd 0604 -d8415a %1 %2
REM This sets the Run bit in the CS8415
ucmd 0440 -d8415a %1 %2
REM This sets the SWCLK bit in the CS8415 to switch to osc when there is no SPDIF source.
ucmd 0180 -d8415a %1 %2
REM  Set the source for the SPDIF SCLK/LRCLK to the ADC SCLK/LRCLK
setpld -w 0d 05 %1 %2
REM  Set the source for the DAO_MCLK to 8415
setpld -w 05 01 %1 %2
REM  Set the direction of the DAO_MCLK as an output from the PLD
setpld -w 06 01 %1 %2
REM Set data source for the CDI Port to SPDIF and SLCK/LRCLK to ADC
setpld -w 07 ca %1 %2
REM Set data source for the DAI Port to ADC2 and SLCK/LRCLK to ADC
setpld -w 08 da %1 %2
REM Set 4392 in control port mode and sets power down bit
ucmd 0530 -d4392 %1 %2
REM Set 4392 in I2S mode
ucmd 0190 -d4392 %1 %2
```

```
REM Set 4392 in control port mode and diables power down bit
ucmd 0520 -d4392 %1 %2
REM This sets I2S in the 8405
ucmd 0504 -d8405a %1 %2
REM This sets the Run bit in the 8405
ucmd 0440 -d8405a %1 %2
```

APPENDIX C: CDB49400.INI

```
# Horizontal Fields:
#       [part] [I2Caddr] [SPIaddr] [SPI CSn]
#      [reset(bit to drop in PLD addr 0x01)]
#                [INTREQ_NUM] [Print Format]
#[Parallel word length] [Parallel CSn]
#[Read_Type]
#
# Vertical Fields:
#board - first non-comment, non-blank line
#parts - other lines
# note: reset can only take on values 01,02
#
# Default is CS4930 interface
#
# INTREQ_NUM is the bit position within the INT register in the PLD
#
# Read_Type can be DSP or normal
#
# Word Length is in bytes
#
# these settings are for J47=hi, J38=lo, J9=lo
CDB49400
8415a 2A 20 02 02 ff 01 00 00 normal
8405a 20 20 06 02 ff 01 00 00 normal
4392  22 20 04 02 ff 01 00 00 normal
DSPC  82 82 01 01 03 04 04 03 DSP
DSPAB  00 00 00 01 02 03 01 00 DSP
default  82 82 01 01 03 04 04 03 DSP
```

APPENDIX D: RESET.BAT

```
echo Reset DSP and board.....

REM Mute the DACs
setpld -w 02 20 %1 %2

REM reset the board (CS8415 shares reset with DACs and ADCs)
urst -d8415a %1 %2

REM reset the DSP
urst -ddspc %1 %2
```

APPENDIX E: BOARD CONTROL SOFTWARE

There is a suite of programs used to control the UDSP from a PC DOS command line.

The software tools are designed to operate from a DOS prompt so that they can be scripted using the MS-DOS batch language. They will work with any of the 3 parallel port addresses (0x378, 0x3bc, 0x278). The default address for all of the programs is 0x378 (typically LPT1), but the port address can be changed by using the '-p' option provided with every tool. Each time a program is executed, the address that was used is echoed to the screen. If a program seems to fail, verification of the parallel port address should the first step in troubleshooting.

All of these programs are designed to access the daughter card connected to the UDSP board using SPI/I^{2}C® serial communication and Intel®/Motorola® parallel communication. The communication mode can be chosen from the command line with the '-m' option. It should be remembered that the mode chosen must correspond to the communication mode used by the devices on the daughter card. If the device on the board is set up for one communication mode and the drivers are used with another, results will be unpredictable. All peripherals on the daughter card are configured for SPI serial communication mode.

The usage of each program will vary, depending on the type of card that is installed. The programs retrieve a valid list of targets for the current card from a file specified in the uINI_path environment variable. This file will list all of the recognized mnemonics for the UDSP parallel port drivers, along with each target's I^{2}C® address, SPI address, chip select number, and reset number (for reset capable devices). It also specifies how messages from the device should be read. For DSP-style reads, the driver will read until the INTREQ line goes high. For non-DSP devices, the read operation will read out 1 byte. Please note that most non-DSP devices require an aborted write operation to properly set the MAP pointer before reading.

The target list file, called CDB49400.INI, must follow a very specific format. An example of this can be found "CDB49400.INI" on page 19.

A list of available drivers and their usage is found below:

UCMD.exe - Send commands or configuration files to a target device.

```
Usage:  ucmd <[ABCDEF..] or [-fX]> [-dZZZZ..] [-mY] [-pWWW] [-v]

       -d = device
       ZZZZ.. = device designator, eg dspab, dspc, 8415a, etc.

       -m = communication mode
       Y = mode designator (i=I2C, s=SPI*, m=MOT, n=INT)

       ABCDEF.. = hex data (1-100 bytes)
       -f = send configuration file
       X = .cfg file containing configuration parameters

       -p = parallel port address
       WWW = address in hex (278, 378* or 3bc)

       -v = enable verbose mode

       * = default value

Example: ucmd 000001 -d4341 -p3bc

Notes:  A configuration file is a list of commands, contained in an ASCII text file. This file
can be any length, and should list the commands in hex, with an even number of characters per
line. Comments can be made in the file by putting a # at the beginning of the line. The entire
line will be interpreted as a comment. Please see the accompanying *.cfg files for examples of
a configuration file.
```

URD.exe - Program used to read back responses from a target device. If the INTREQ pin is not low when URD.exe is executed, the program will wait until INTREQ drops. Press the 'Enter' key to exit the read wait loop.

```
Usage: urd [-dZZZZ..] [-mY] [-pXXX] [-v] [-h]

       -d = device
       ZZZZ = device designator, eg dspab, dspc, 8415a, etc.

       -m = communication mode
       Y = mode designator (i=I2C, s=SPI*, m=MOT, n=INT)

       -p = parallel port address
       XXX = address in hex (278, 378* or 3bc)

       -v = enable verbose mode

       -h = this message

       * = default value

EXAMPLE: urd -d4940c -p378

Notes: If the associated INTREQ pin is not low when URD is executed, the program will wait
until INTREQ drops for DSP devices ONLY. Press the 'Enter' key to exit the read wait loop in
this case.
```

URST.exe - Program used to perform hard reset or soft reset on the target device.

```
Usage:     urst [-dZZZZ..] [-mY] [-s] [-pXXX] [-v] [-h]

       -d = device
       ZZZZ = device designator, eg dspab, dspc, 8415a

       -m = communication mode
       Y = mode designator (i = I2C, s = SPI*, n = INTEL, m = MOTOROLA)

       -s = Soft Reset

       -p = parallel port address
       XXX = address in hex (278, 378* or 3bc)

       -v = enable verbose mode

       -h = this message

       * = default value
```

U40LD.exe - Program used to load code onto a DSP.

```
Usage: u40ld <dspab_input_file.uld> <dspc_input_file.uld> [-mY] [-pXXX] [-v]

       -m = communication mode
       Y = mode designator (i = I2C, s = SPI*, n = INTEL, m = MOTOROLA)

       -p = parallel port address
       XXX = address in hex (278, 0x378* or 0x3bc)

       -v = disable verbose mode

       * = default value
```

SetPLD.exe - Program used to read and write PLD registers.

```
Usage: setpld -r/-w RR [DD]
       Where -r is to read from register RR, -w is to write data DD into register RR. RR and DD
are in hex.
```

APPENDIX F: INSTALLATION OF BOARD CONTROL SOFTWARE

The UDSP PC driver utility set comes in two versions. The Direct Hardware version will communicate directly with the PC's parallel port to control the UDSP board. The DLPortIO version uses the DLPortIO driver to access the parallel port on hardware protected operating systems.

In general, direct hardware capable operating systems (such as Microsoft® Windows 95®, Windows 98®, and Windows ME®) allow any program to directly control any of the PC's peripherals. With the UDSP board, this allows for faster interface speeds (up to 4 times faster).

For protected operating systems (such as Microsoft® Windows NT®, Windows 2000®, and Windows XP®), the UDSP driver set requires the use of the DLPortIO driver. This utility allows the UDSP drivers to access the parallel port safely.

The UDSP driver set requires bidirectional communication with the UDSP board, and hence a bidirectional capable parallel port is needed. An ECP-type port is required. Please note that an SPP-type port will not work with the UDSP board. The type and location (I/O address) of the parallel port installed can be found in the Windows Control Panel (please see Windows Help for more information on these settings). The UDSP drivers assume by default that the parallel port address is 0x378. Other ports may be used with the -pXXX option, where XXX is 3bc or 278.

Installation on Microsoft® Windows 95®, 98®, ME® and other direct hardware capable Windows® versions

1. Copy the contents of the *udsp_1-4-directhw directory* to a suitable location. The folder c:\udsp is recommended.

2. Copy the contents of *cs49400 directory* to c:\cs49400.

3. Edit your c:\autoexec.bat file to include the path to the UDSP drivers. This will allow you to use the drivers in any directory without specifying the path to the executables. The following line should be added: "set PATH=*your_path*;%PATH%;", where *your_path* the directory chosen in step 1.

4. Again, edit your c:\autoexec.bat file to add the line "set uINI_PATH=*your_CDB_path\CDB49400.ini*", where *your_CDB_path* is the folder chosen in step 2. For the folder c:\cs49400\cdb49400 this would read "set uINI_PATH=c:\cs49400\cdb49400\CDB49400.ini". This will allow the drivers to locate the CDB49400 configuration file, which contains information about the various devices on this board.

5. For the previous few steps to have an effect on your computer (for the drivers to be available in any DOS window in any location), you will need to reboot it at this time.

The UDSP drivers have now been successfully installed. The CDB49400 kit is now ready for use. Several demonstration batch files (*.bat) are available in the CDB49400\Configs directory. Please see the"Quick Start" on page 4 for information on the use of these batch files.

Installation on Microsoft® Windows NT®, Windows 2000®, and Windows XP® and other protected Windows® versions

1. Install the DLPortIO driver included with the CDB49400 driver kit. This can be done by running the program *port95nt.exe* and following the instructions given.

2. Copy the contents of *udsp_1-5-dlportio directory* to a suitable location. The folder c:\udsp is recommended.

3. Copy the contents of *cs49400* directory to c:\cs49400.

4. Edit your c:\autoexec.bat file to include the path to the UDSP drivers. This will allow you to use the drivers in any directory without specifying the path to the executables. The following line should be added: "set PATH=*your_path*;%PATH%;", where *your_path* is the directory chosen in step 1.

5. Again, edit your c:\autoexec.bat file to add the line "set uINI_PATH=*your_CDB_path\CDB49400.ini*", where *your_CDB_path* is the folder chosen in step 2. For the folder c:\cs49400\cdb49400 this would read "set uINI_PATH=c:\cs49400\cdb49400\CDB49400.ini". This will allow the drivers to locate the CDB49400 configuration file, which contains information about the various devices on this board.

6. For the previous few steps to have an effect on your computer (for the drivers to be available in any DOS window in any location), you will need to reboot it at this time.

The UDSP drivers have now been successfully installed. The CDB49400 kit is now ready for use. Several demonstration batch files (*.bat) are available in the CDB49400\Configs directory. Please see "Quick Start" on page 4 for information on the use of these batch files.

APPENDIX G: CDB49400 SCHEMATICS

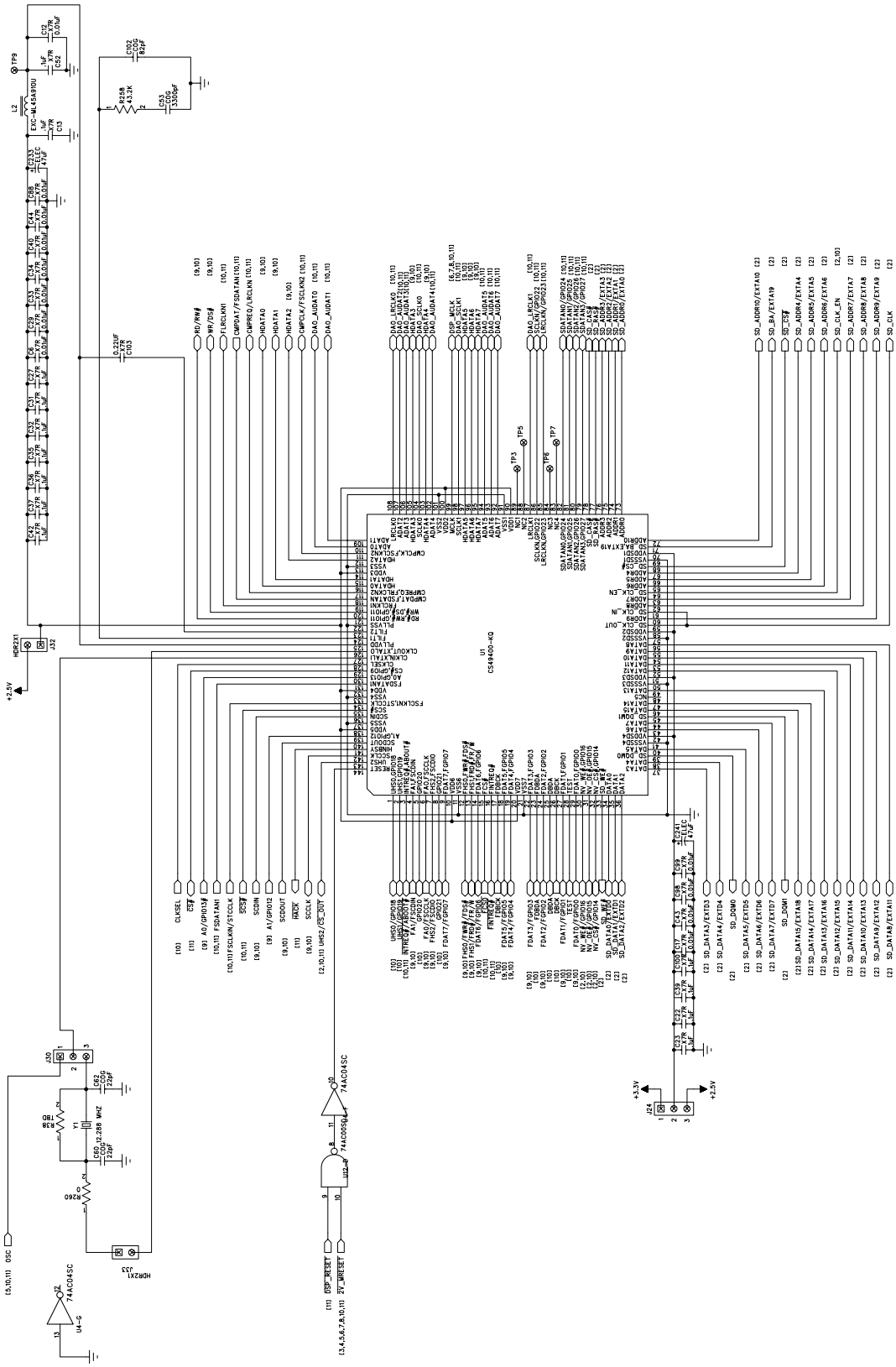


Figure 4. Sheet 1 - DSP

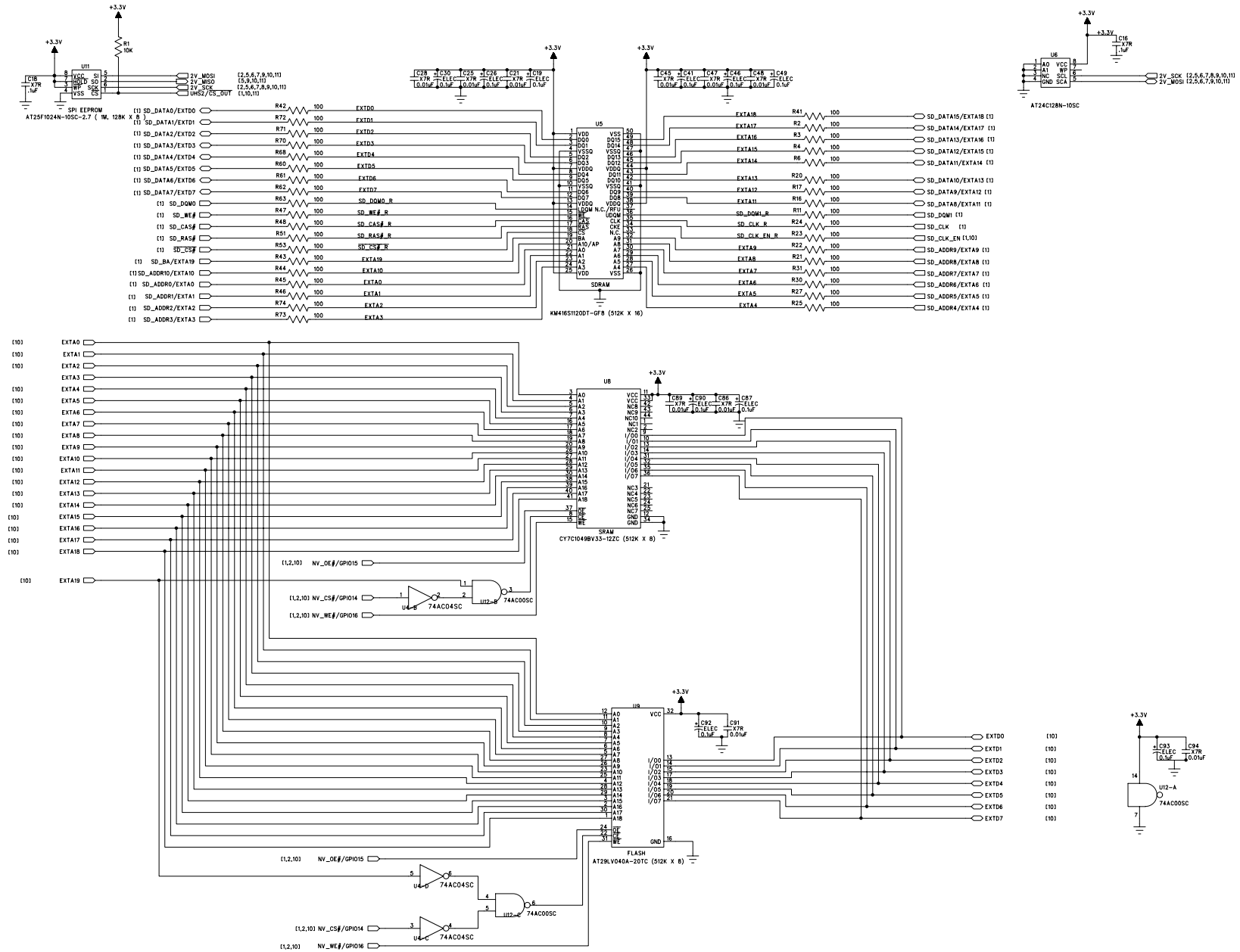


Figure 5. Sheet 2 - Memory

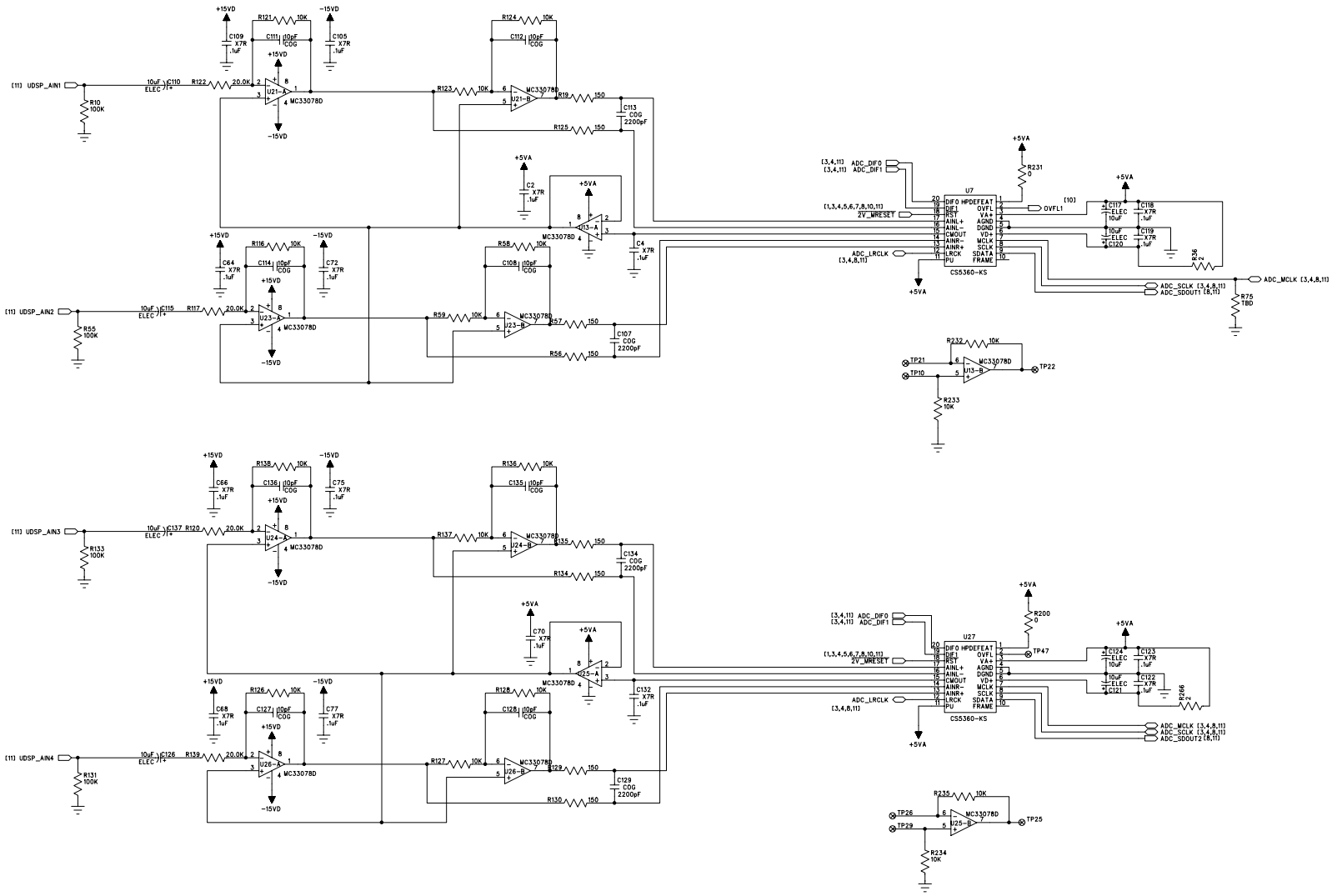


Figure 6. Sheet 3 - ADC - 1

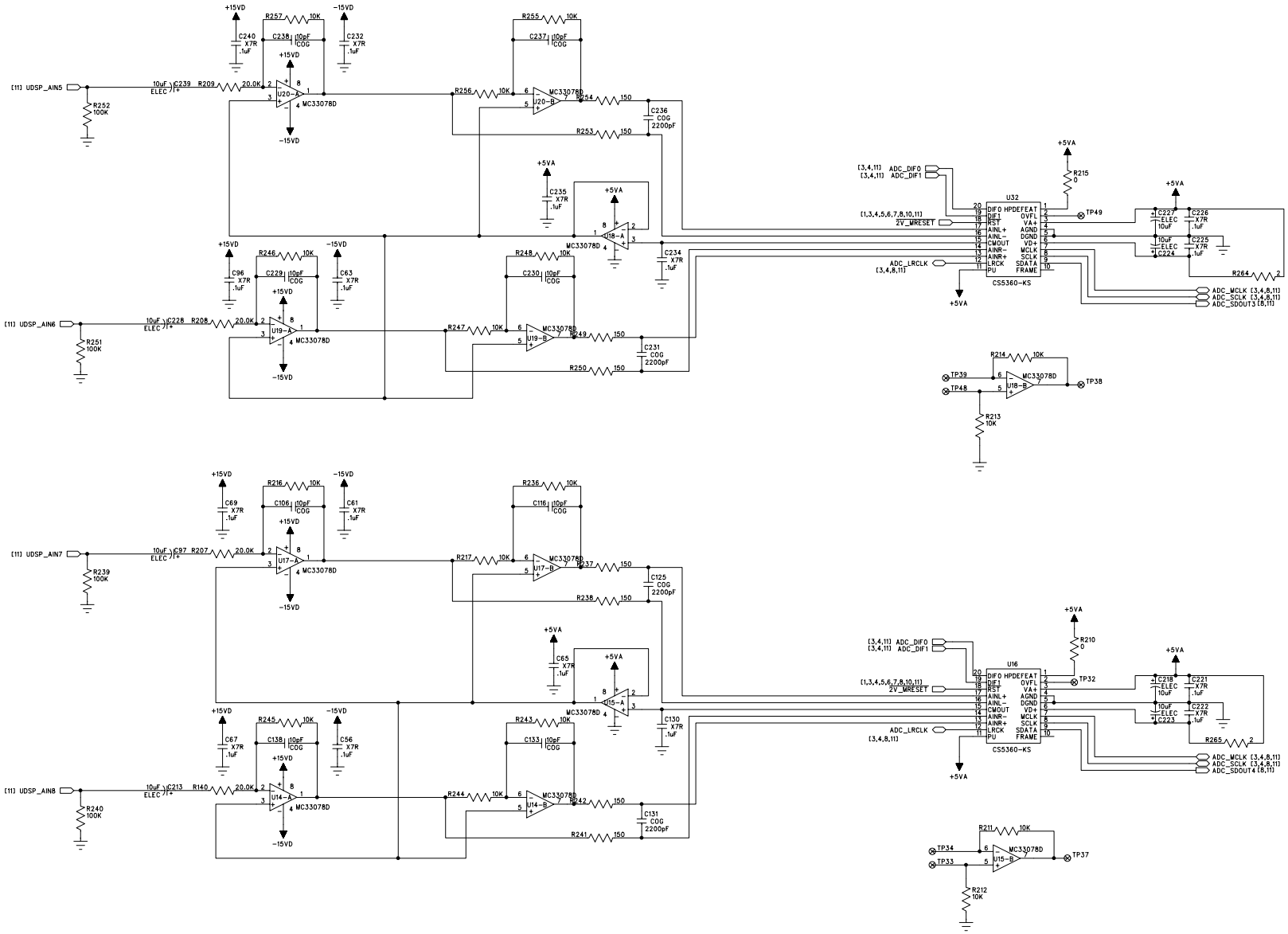


Figure 7. Sheet 4 - ADC - 2

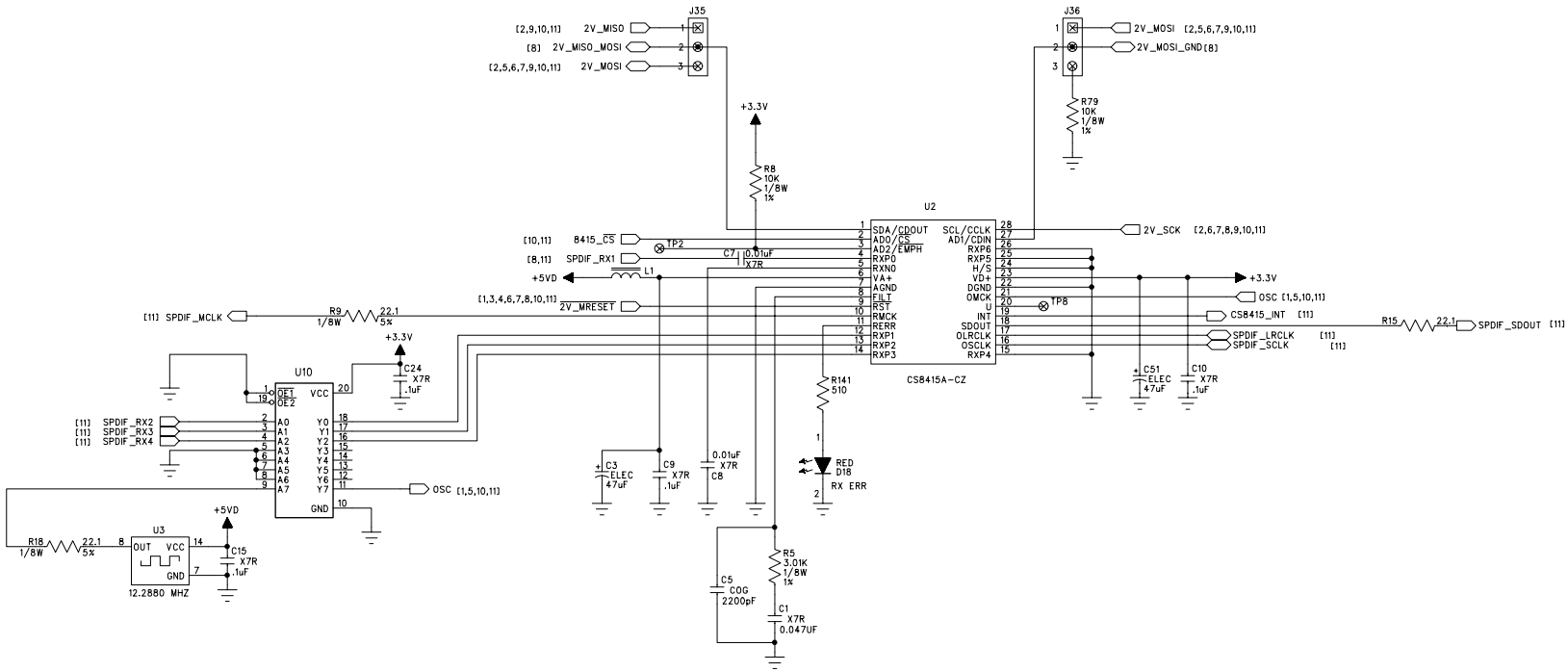


Figure 8. Sheet 5 - S/PDIF RCVR

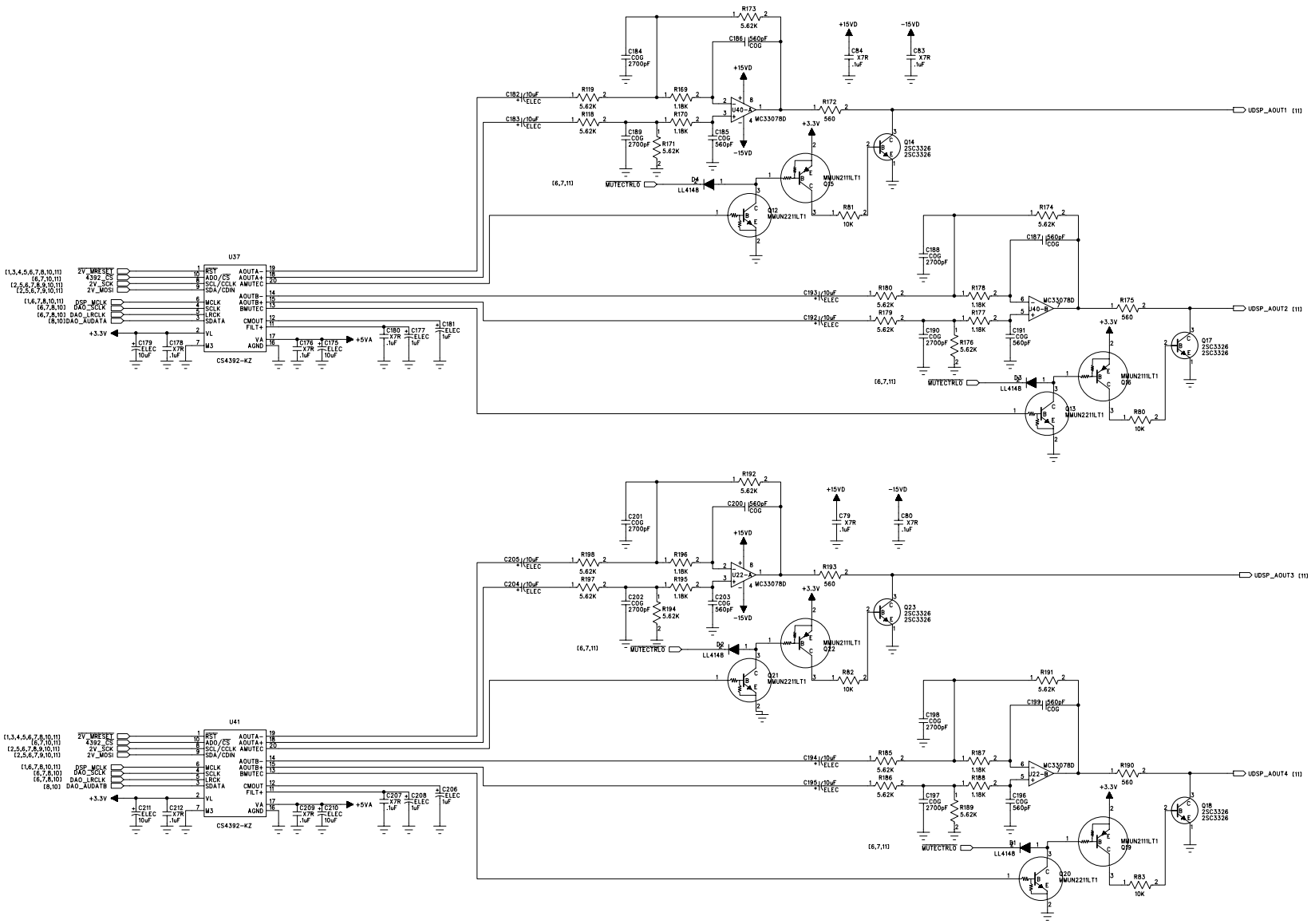


Figure 9. Sheet 6 - DAC - 1

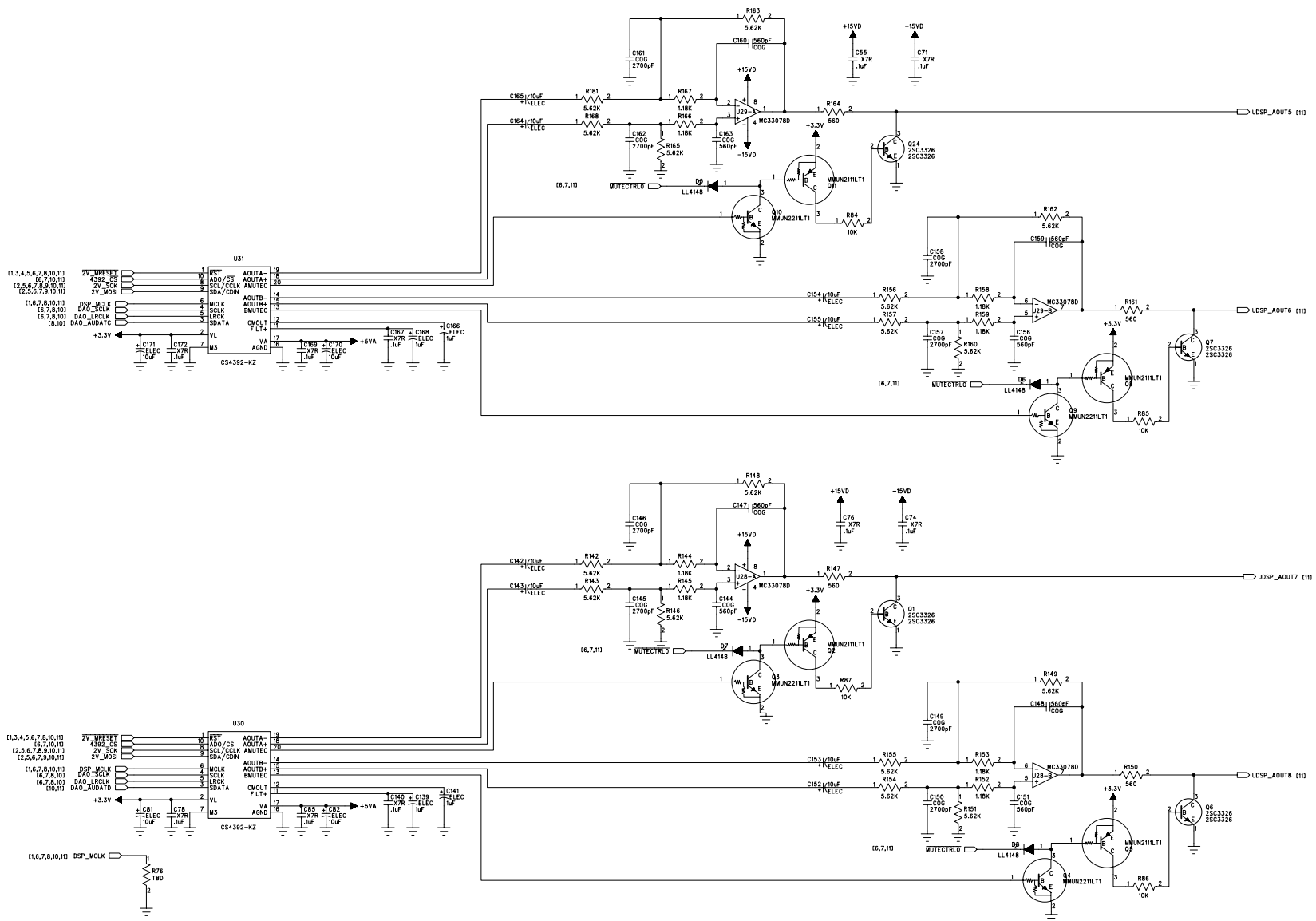


Figure 10. Sheet 7 - DAC - 2

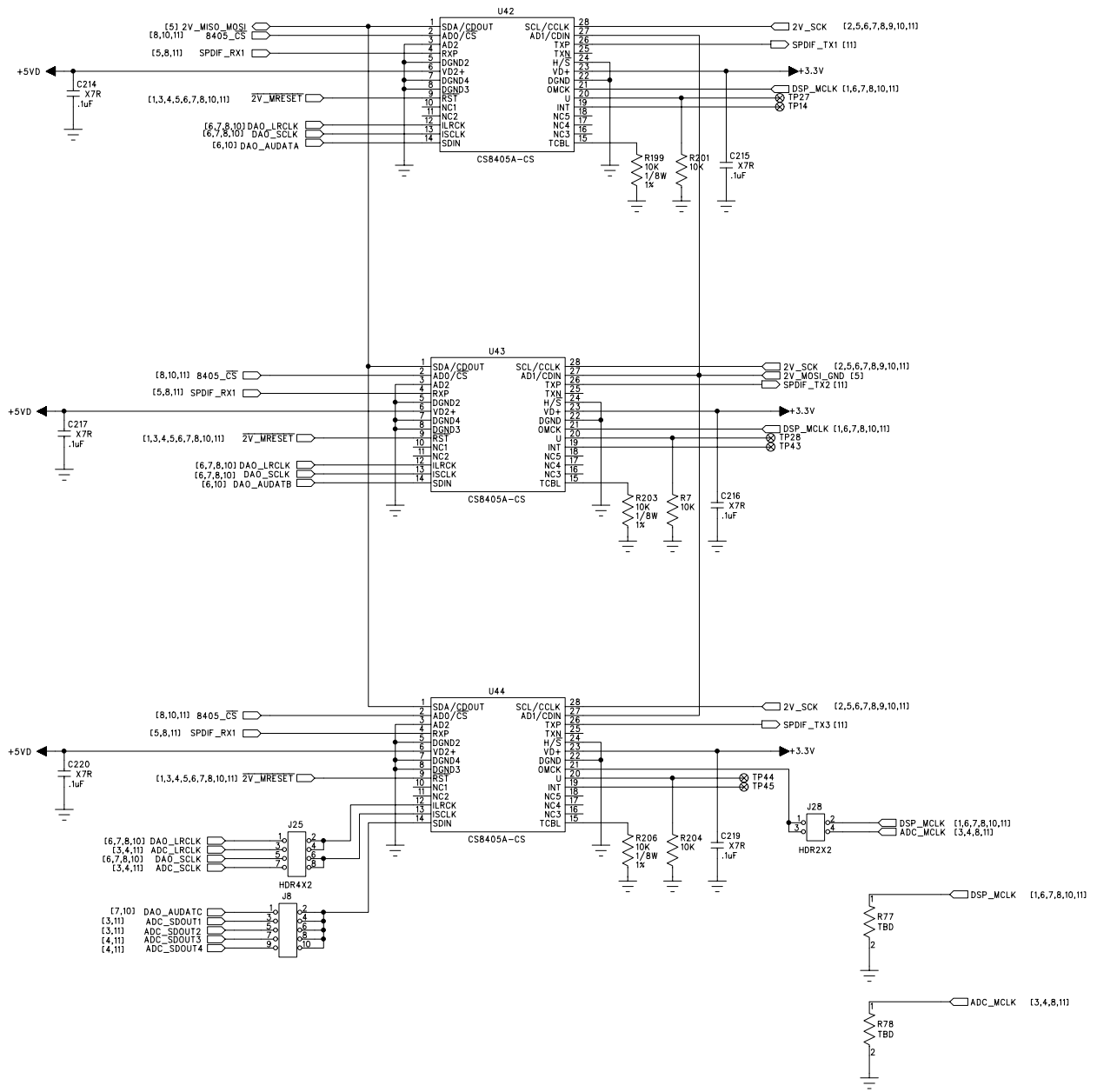


Figure 11. Sheet 8 - S/PDIF XCVR

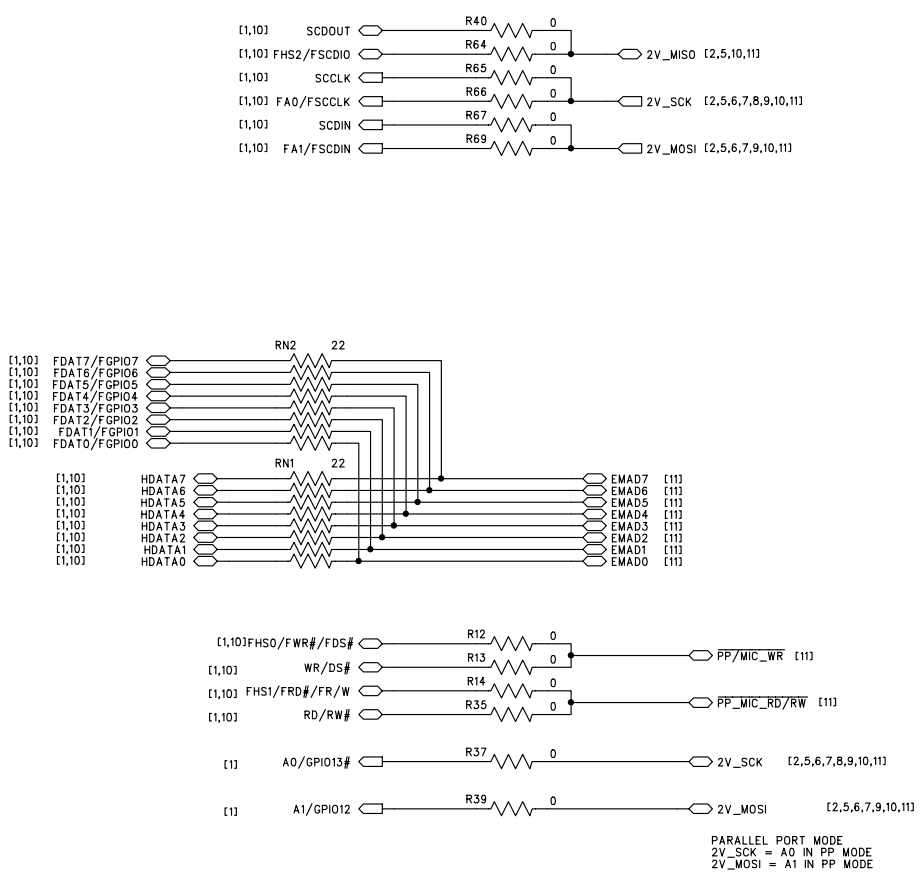
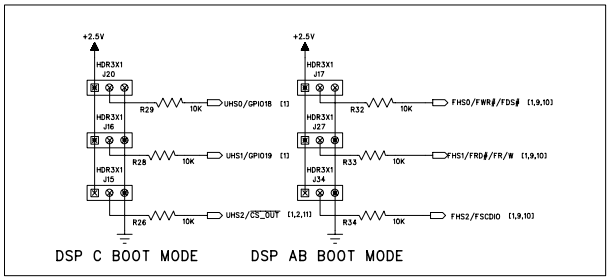
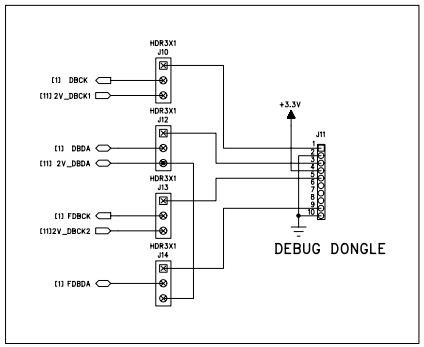
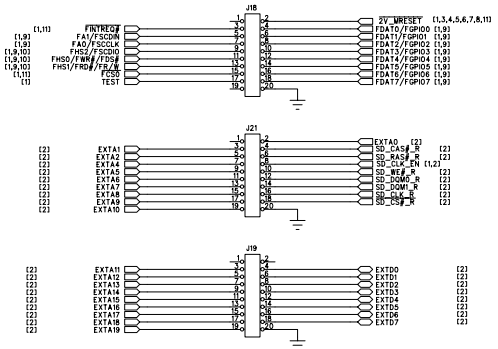
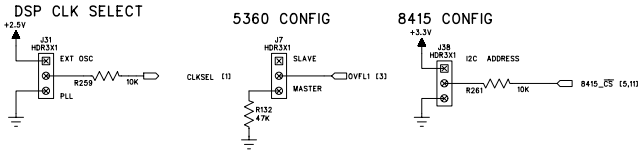


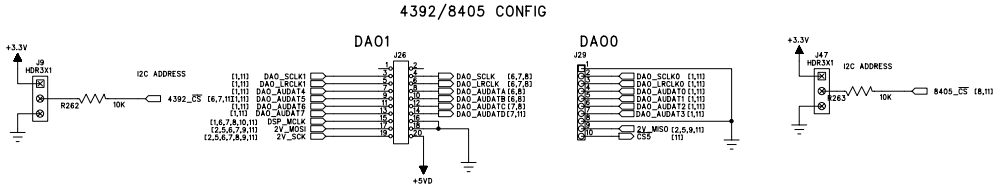
Figure 12. Sheet 9 - Buffers











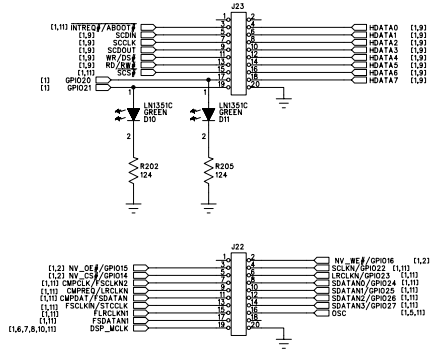


Figure 13. Sheet 10 - Configs.

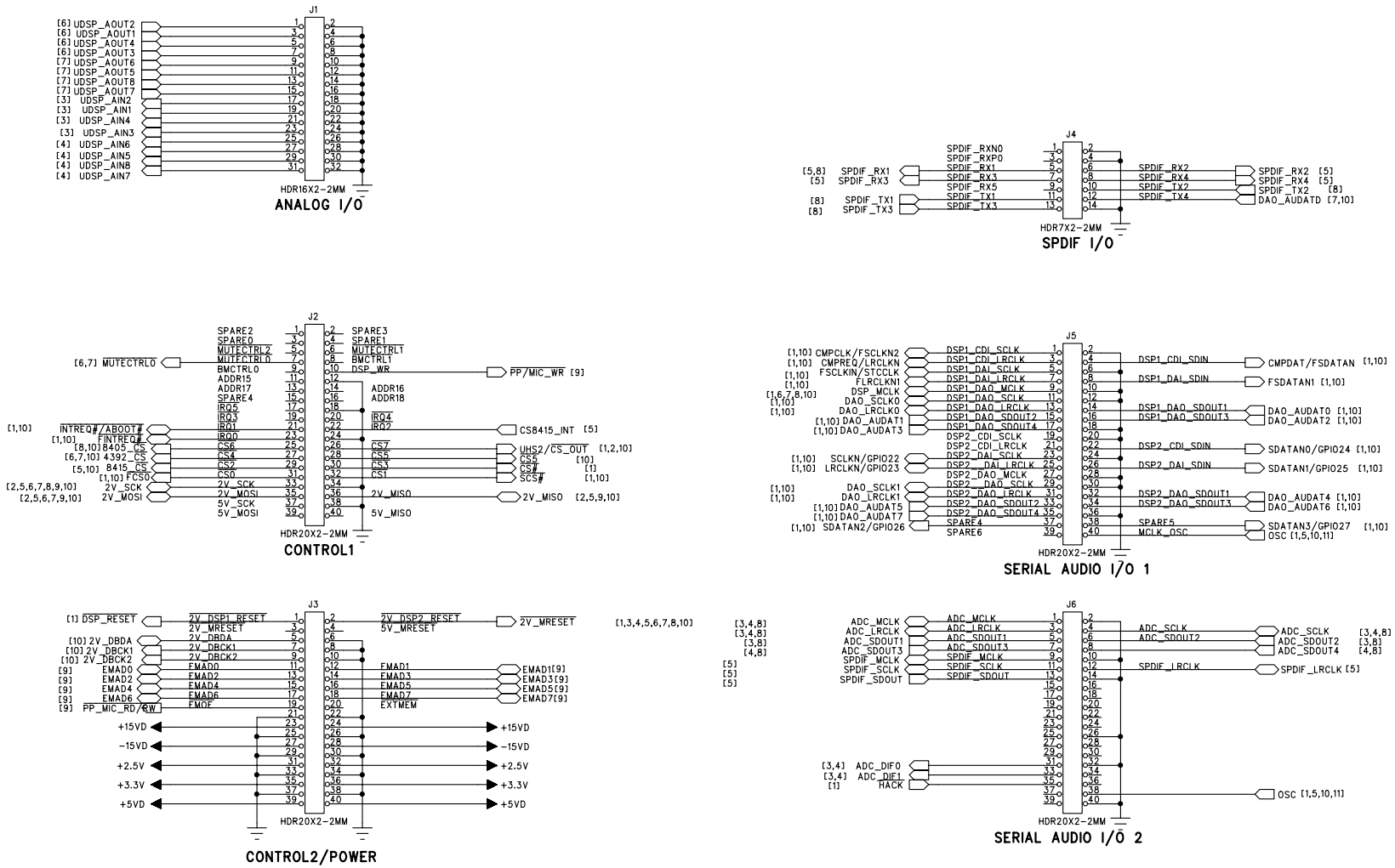


Figure 14. Sheet 11 - UDSP Interface.

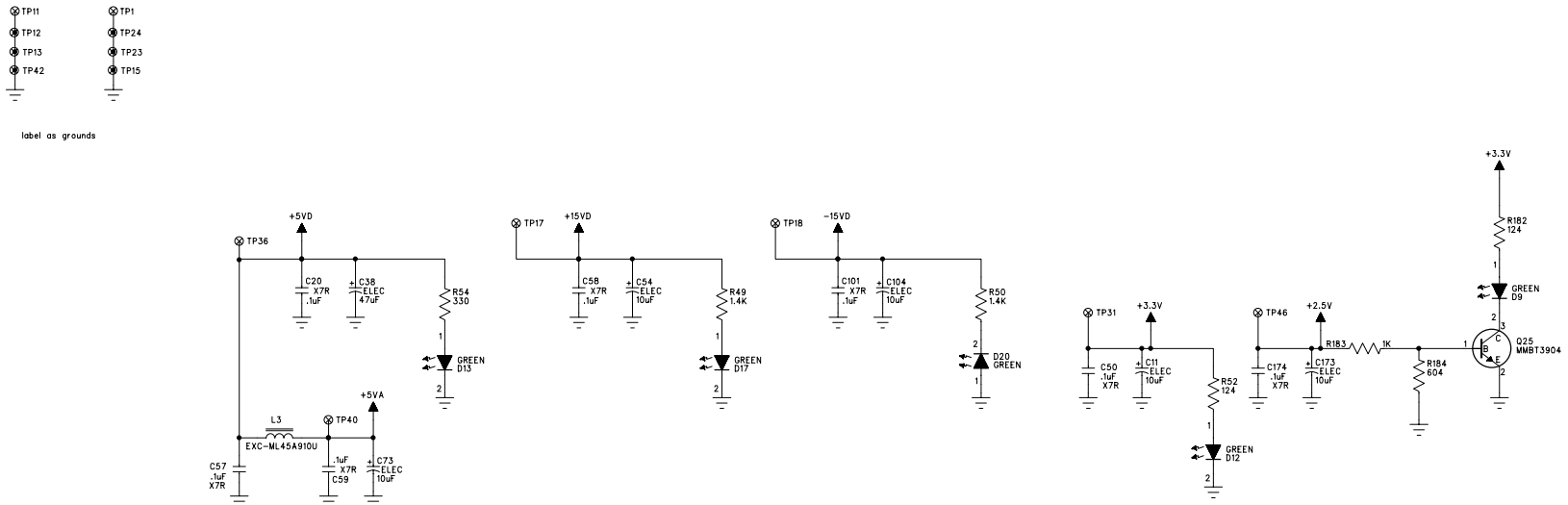


Figure 15. Sheet 12 - Power Supplies

APPENDIX H: BILL OF MATERIALS -CDB49400

Item	Qty	Reference	Part Number	Manufacturer	Description
1	1	C1	C0805C473J5RAC	KEMET	CAP 0.047UF X7R 0805 50V 5%
2	85	C2 C4 C9 C10 C13 C14 C15 C16 C18 C20 C22 C23 C24 C27 C31 C32 C35 C36 C37 C39 C42 C50 C52 C55 C56 C57 C58 C59 C61 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C74 C75 C76 C77 C78 C79 C80 C83 C84 C85 C96 C100 C101 C105 C109 C118 C119 C122 C123 C130 C132 C140 C167 C169 C172 C174 C176 C178 C180 C207 C209 C212 C214 C215 C216 C217 C219 C220 C221 C222 C225 C226 C232 C234 C235 C240	C0805C104K5RAC	KEMET	CAP 0.1UF X7R 0805 50V 10%
3	5	C3 C38 C51 C233 C241	ECE-V1VA470WP	PANASONIC	CAP 47uF ELEC VS SERIES SMT CASE-D 35V 20%
4	1	C5	C1206C222J5GAC	KEMET	CAP 2200PF COG 1206 50V 5%
5	24	C6 C7 C8 C12 C17 C21 C25 C28 C29 C33 C34 C40 C43 C44 C45 C47 C48 C86 C88 C89 C91 C94 C98 C99	C0805C103J5RAC	KEMET	CAP 0.01UF X7R 0805 50V 5%
6	5	C11 C54 C73 C104 C173	ECE-V1VA100P	PANASONIC	CAP 10uF ELEC VA SERIES SMT CASE-C 35V 20%
7	10	C19 C26 C30 C41 C46 C49 C87 C90 C92 C93	ECE-V1HA0R1R	PANASONIC	CAP 0.1uF ELEC VA SERIES SMT CASE-B 50V 20%
8	1	C53	C1206C332J5GAC	KEMET	CAP 3300PF COG 1206 50V 5%
9	2	C60 C62	C0805C220J5GAC	KEMET	CAP 22PF COG 0805 50V 5%
10	40	C81 C82 C97 C110 C115 C117 C120 C121 C124 C126 C137 C142 C143 C152 C153 C154 C155 C164 C165 C170 C171 C175 C179 C182 C183 C192 C193 C194 C195 C204 C205 C210 C211 C213 C218 C223 C224 C227 C228 C239	ECE-V1CA100R	PANASONIC	CAP 10uF ELEC VA SERIES SMT CASE-B 16V 20%
11	1	C102	C0805C820J5GAC	KEMET	CAP 82PF COG 0805 50V 5%

Item	Qty	Reference	Part Number	Manufacturer	Description
12	1	C103	C1206C224J5RAC	KEMET	CAP 0.22UF X7R 1206 50V 5%
13	16	C106 C108 C111 C112 C114 C116 C127 C128 C133 C135 C136 C138 C229 C230 C237 C238	C0805C100J5GAC	KEMET	CAP 10pF COG 0805 50V 5%
14	8	C107 C113 C125 C129 C131 C134 C231 C236	C0805C222J5GAC	KEMET	CAP 2200PF COG 0805 50V 5%
15	8	C139 C141 C166 C168 C177 C181 C206 C208	ECE-V1HS010SR	PANASONIC	CAP 1uF ELEC VS SERIES SMT CASE-A 50V 20%
16	16	C144 C147 C148 C151 C156 C159 C160 C163 C185 C186 C187 C191 C196 C199 C200 C203	C0805C561J5GAC	KEMET	CAP 560PF COG 0805 50V 5%
17	16	C145 C146 C149 C150 C157 C158 C161 C162 C184 C188 C189 C190 C197 C198 C201 C202	C1206C272J5GAC	KEMET	CAP 2700PF COG 1206 50V 5%
18	8	D1 D2 D3 D4 D5 D6 D7 D8	LL4148DI	DIODES INC	GENERAL PURPOSE SIGNAL DIODE SOD-80
19	7	D9 D10 D11 D12 D13 D17 D20	LN1351C	PANASONIC	LED SMT 3216 GREEN
20	1	D18	LN1251C	PANASONIC	LED SMT 3216 RED
21	1	J1	87089-3216	MOLEX	STAKE HEADER 2MM PITCH 16X2
22	4	J2 J3 J5 J6	87089-4016	MOLEX	STAKE HEADER 2MM PITCH 20X2
23	1	J4	87089-1417	MOLEX	STAKE HEADER 2MM PITCH 7X2
24	19	J7 J9 J10 J12 J13 J14 J15 J16 J17 J20 J24 J27 J30 J31 J34 J35 J36 J38 J47	TSW-07-103-G-S	SAMTEC	STAKE HEADER 3X1 0.1"" CTR GOLD
25	1	J8	TSW-105-07-G-D	SAMTEC	STAKE HEADER 5X2 0.1""CTR GOLD
26	2	J11 J29	TSW-110-07-G-S	SAMTEC	HEADER 10X1 0.1""CTRS GOLD
27	6	J18 J19 J21 J22 J23 J26	TSW-110-07-G-D	SAMTEC	HEADER 10X2 0.1"" CTR GOLD
28	1	J25	TSW-104-07-G-D	SAMTEC	STAKE HEADER 4X2 0.1"" CTR GOLD
29	1	J28	TSW-102-07-G-D	SAMTEC	STAKE HEADER 2X2 0.1"" CTR GOLD
30	2	J32 J33	TSW-102-07-G-S	SAMTEC	STAKE HEADER 2X1 0.1""CTR GOLD
31	3	L1 L2 L3	EXC-ML45A910U	PANASONIC	FERRITE BEAD 1806
32	8	Q1 Q6 Q7 Q14 Q17 Q18 Q23 Q24	2SC3326	TOSHIBA	TRANSISTOR NPN EPITAXIAL TYPE SC59

Item	Qty	Reference	Part Number	Manufacturer	Description
33	8	Q2 Q5 Q8 Q11 Q15 Q16 Q19 Q22	MMUN2111LT1	MOTOROLA	TRANSISTOR PNP SILICON SMT WITH MONO-LITHIC BIAS RES NET SOT23
34	8	Q3 Q4 Q9 Q10 Q12 Q13 Q20 Q21	MMUN2211LT1	MOTOROLA	TRANSISTOR NPN SILICON TRANSISTOR WITH MONOLITHIC BIAS RES NET S0T23
35	1	Q25	MMBT3904LT1	MOTOROLA	TRANSISTOR NPN SOT23
36a	6	R26 R28 R29 R32 R33 R34	CRCW08053301F	DALE	. 100ppmDALERANSISTOR NPN SOT23
36	59	R1 R7 R8 R58 R59 R79 R80 R81 R82 R83 R84 R85 R86 R87 R116 R121 R123 R124 R126 R127 R128 R136 R137 R138 R199 R201 R203 R204 R206 R211 R212 R213 R214 R216 R217 R232 R233 R234 R235 R236 R243 R244 R245 R246 R247 R248 R255 R256 R257 R259 R261 R262 R263	CRCW08051002F	DALE	RES 10K 0805 1/10W 1%. 100ppmDALE
37	36	R2 R3 R4 R6 R11 R16 R17 R20 R21 R22 R23 R24 R25 R27 R30 R31 R41 R42 R43 R44 R45 R46 R47 R48 R51 R53 R60 R61 R62 R63 R68 R70 R71 R72 R73 R74	CRCW06031000F	DALE	RES 100-OHM 0603 1/16W 1% 200ppm
38	1	R5	CRCW08053011F	DALE	RES 3.01K 0805 1/10W 1%. 100ppm
39	3	R9 R15 R18	CRCW080522R1F	DALE	RES 22.1 OHMS 0805 1/10W 1%. 100ppm
40	8	R10 R55 R131 R133 R239 R240 R251 R252	CRCW08051003F	DALE	RES 100K 0805 1/10W 1%. 100ppm
41	17	R12 R13 R14 R35 R37 R39 R40 R64 R65 R66 R67 R69 R200 R210 R215 R231 R260	CRCW0805000FT	DALE	RES 0 0805 1/10W
42	16	R19 R56 R57 R125 R129 R130 R134 R135 R237 R238 R241 R242 R249 R250 R253 R254	CRCW08051500F	DALE	RES 150 OHMS 0805 1/10W 1%. 100ppm
43	4	R36 R264 R265 R266	CRCW12062R0J	DALE	RES 2 OHMS 1206 1/8W 5% 300ppm
44	5	R38 R75 R76 R77 R78	TBD	DALE	RES TBD 0805 1/8W 1% 100ppm
45	2	R49 R50	CRCW08051401FT	DALE	RES 1.4K 0805 1/10W 1% 100ppm
46	4	R52 R182 R202 R205	CRCW08051240F	DALE	RES 124 OHMS 0805 1/10W 1%. 100ppm
47	1	R54	CRCW12063300F	DALE	RES 330 1206 1/10W 1% 100ppm

Item	Qty	Reference	Part Number	Manufacturer	Description
48	7	R117 R120 R122 R140 R207 R208 R209	CRCW08052002F	DALE	RES 20.0K 0805 1/10W 1%. 100ppm
49	32	R118 R119 R142 R143 R146 R148 R149 R151 R154 R155 R156 R157 R160 R162 R163 R165 R168 R171 R173 R174 R176 R179 R180 R181 R185 R186 R189 R191 R192 R194 R197 R198	CRCW08055621F	DALE	RES 5.62K 0805 1/10W 1%. 100ppm
50	1	R132	CRCW0805473J	DALE	RES 47K 0805 1/8W 5% 200ppm
51	1	R139	CRCW06032002F	DALE	RES 20.0K 0603 1/16W 1% 200ppm
52	1	R141	CRCW1206511J	DALE	RES 510 1206 1/8W 5% 200ppm
53	16	R144 R145 R152 R153 R158 R159 R166 R167 R169 R170 R177 R178 R187 R188 R195 R196	CRCW08051181F	DALE	RES 1.18K 0805 1/10W 1%. 100ppm
54	8	R147 R150 R161 R164 R172 R175 R190 R193	CRCW08055600F	DALE	RES 560 0805 1/10W 1% 100ppm
55	1	R183	CRCW08051001F	DALE	RES 1K 0805 1/10W 1%. 100ppm
56	1	R184	CRCW08056040F	DALE	RES 604 OHMS 0805 1/10W 1%. 100ppm
57	1	R258	CRCW08054322F	DALE	RES 43.2K 0805 1/10W 1%. 100ppm
58	2	RN1 RN2	4816P-T01-220	BOURNS	RES NETWORK 22 8 ISOLATED SO16-220
59	42	TP1 TP2 TP3 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP17 TP18 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP31 TP32 TP33 TP34 TP36 TP37 TP38 TP39 TP40 TP42 TP43 TP44 TP45 TP46 TP47 TP48 TP49			.062 PAD.042 HOLE NO POP
60	1	U1	IC149-144-145-S5	YAMAICHI	SOCKET QFP PROTOTYPING SMT SOCKET WITH POS. PIN SOLDER TAB
61	1	U2	CS8415-CZ	CIRRUS LOGIC	IC S/PDIF RECEIVER TSSOP28-173
62	1	U3	CX21AF-12.2880MHZ	CAL CRYSTAL	CLOCK OSCILLATOR 12.288MHZ FULL SIZE CASE
63	1	U4	74AC04SC	FAIRCHILD	IC HEX INVERTERS SOIC-150
64	1	U5	KM416S1120DT-GF8	SAMSUNG	IC SDRAM 512K X 16 TSOP 50

Item	Qty	Reference	Part Number	Manufacturer	Description
65	1	U6	AT24C128N-10SC	ATMEL	IC 2-WIRE SERIAL EEPROM 128K SO8-150
66	4	U7 U16 U27 U32	CS5360-KS	CRYSTAL SEMICONDUC-TOR	IC 24 BIT STEREO ADC CONVERTER FOR DIGITAL AUDIO SSOP20-209
67	1	U8	CY7C1049BV33-12ZC	CYPRESS	IC SRAM (512X8) TSOP
68	1	U9	AT29LV040A-20TC	ATMEL	IC FLASH MEMORY (512X8). PLCC32
69	1	U10	SN74HC541DW	TEXAS INST	OCTAL BUFFERS AND LINE DRIVERS SO20-300
70	1	U11	AT25F1024N-10SC-2.7	ATMEL	SPI SERIAL EEPROM IM BIT SO8-150
71	1	U12	74AC00SC	FAIRCHILD	QUAD 2-INPUT POS-NAND GATES SOIC-150
72	16	U13 U14 U15 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26 U28 U29 U40	MC33078D	MOTOROLA	IC DUAL LOW NOISE OP-AMP SO8-150
73	4	U30 U31 U37 U41	CS4392-KZ	CRYSTAL SEMICONDUC-TOR	IC 24 BIT 192KHZ STEREO DAC WITH VOLUME CONTROL TSSOP20-173
74	3	U42 U43 U44	CS8405A-CZ	CIRRUS LOGIC	IC S/PDIF TRANSMITTER TSSOP27-173
75	1	Y1	CCL-6S-12.288C5XFC	CAL CRYSTAL	CRYSTAL PARALLEL CUT 12.288MHZ 20PF HC49S
76	1		CDB49400B.0	Cirrus Logic	PRINTED CIRCTUIT BOARD
77	1		UDSP-1	Cirrus Logic	Assy, Universal DSP Development platform

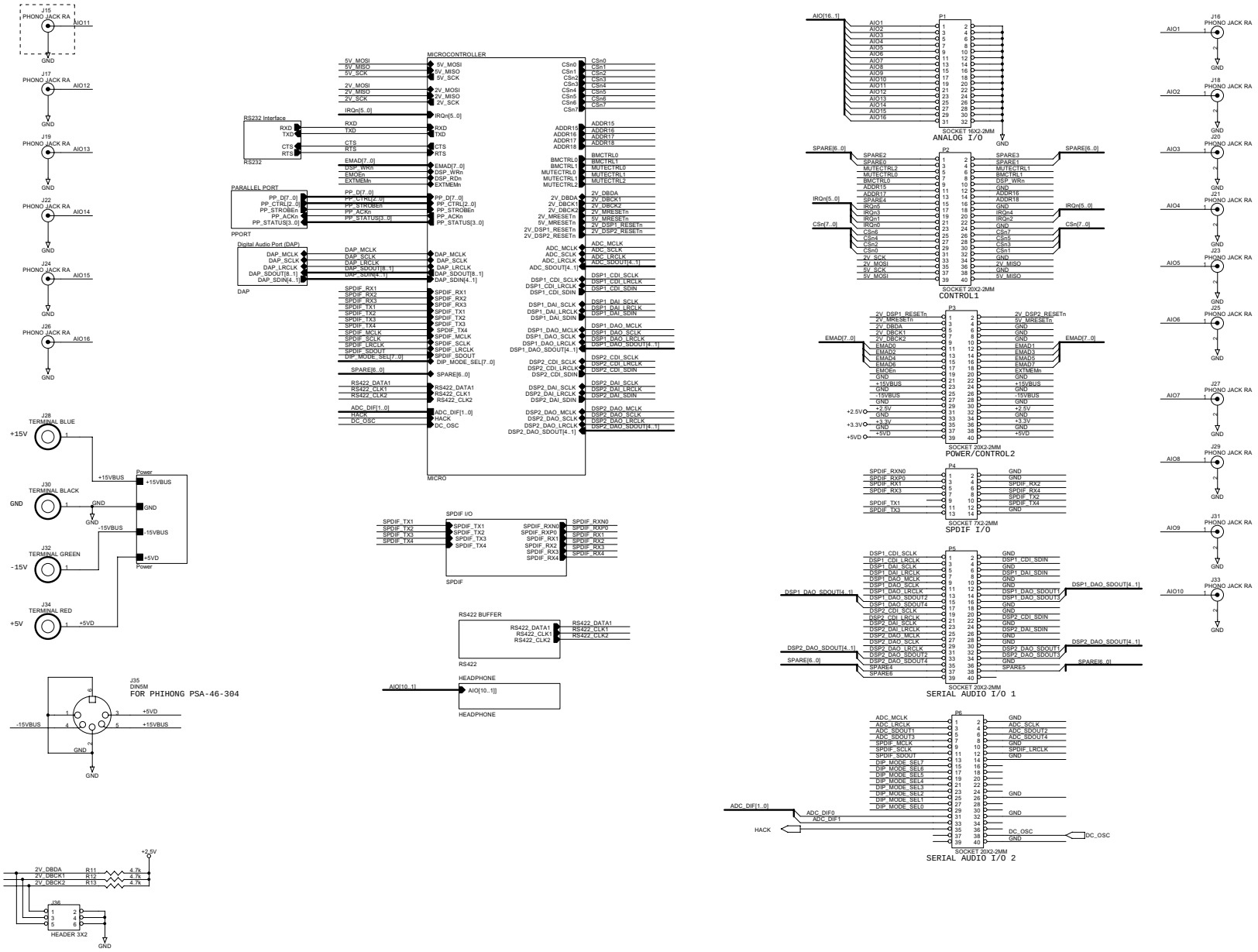


Figure 16. Sheet 1 - Universal DSP System Platform

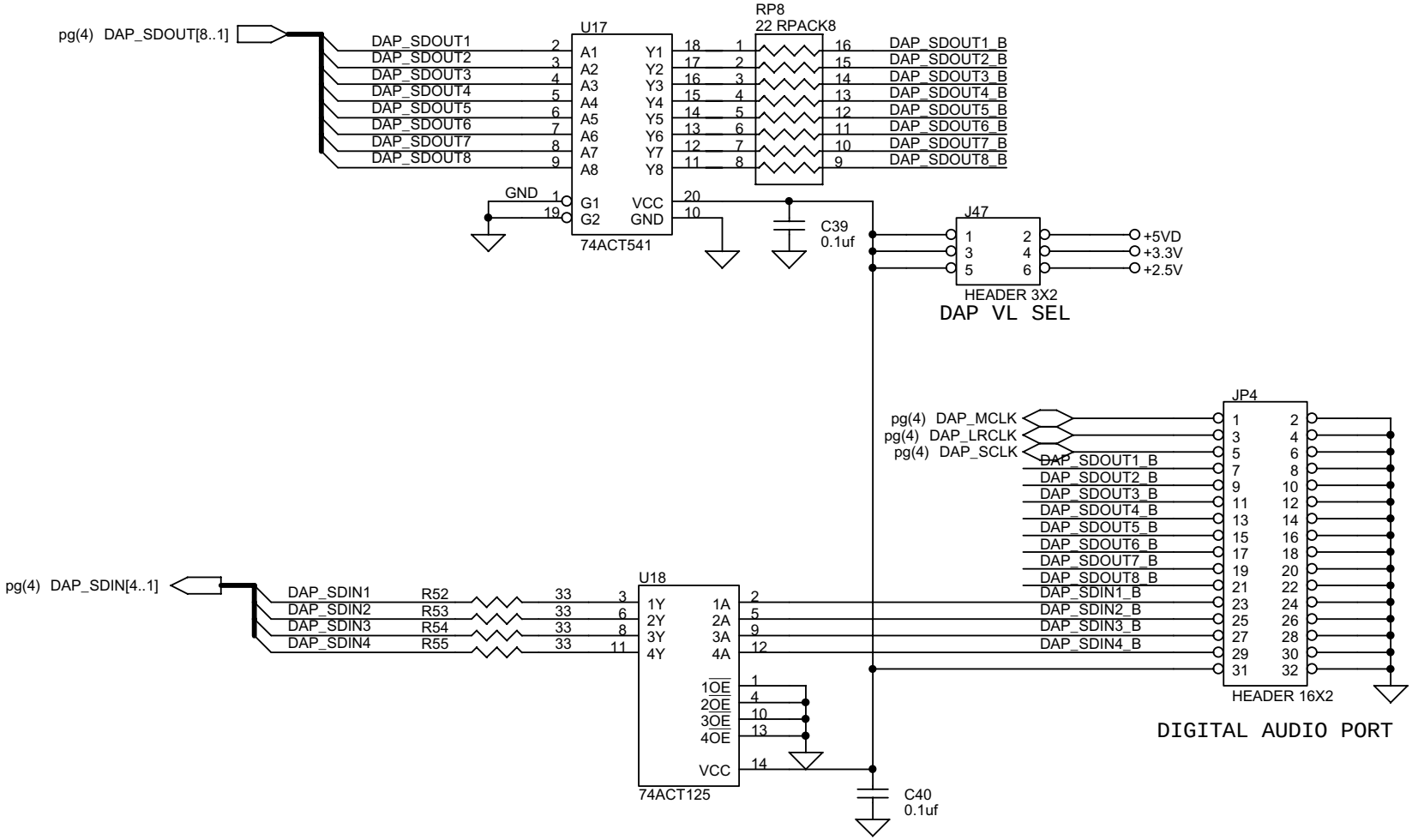


Figure 17. Sheet 2 - Digital Audio Port

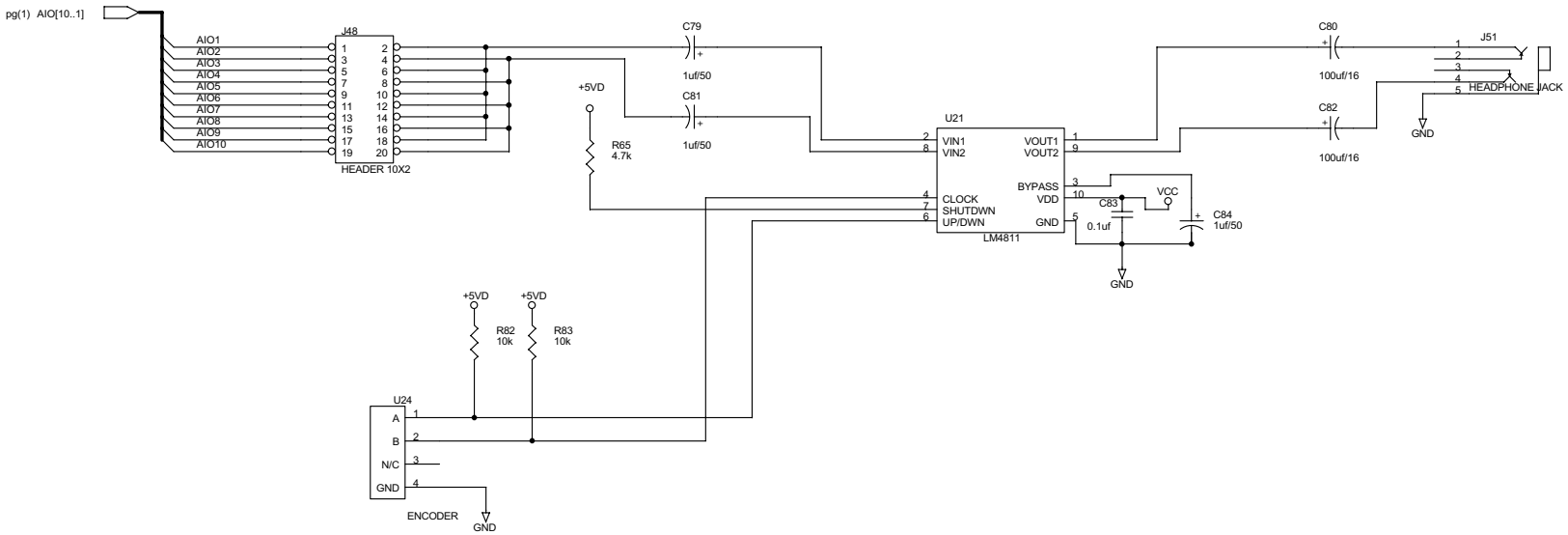


Figure 18. Sheet 3 - Headphone Amplifier

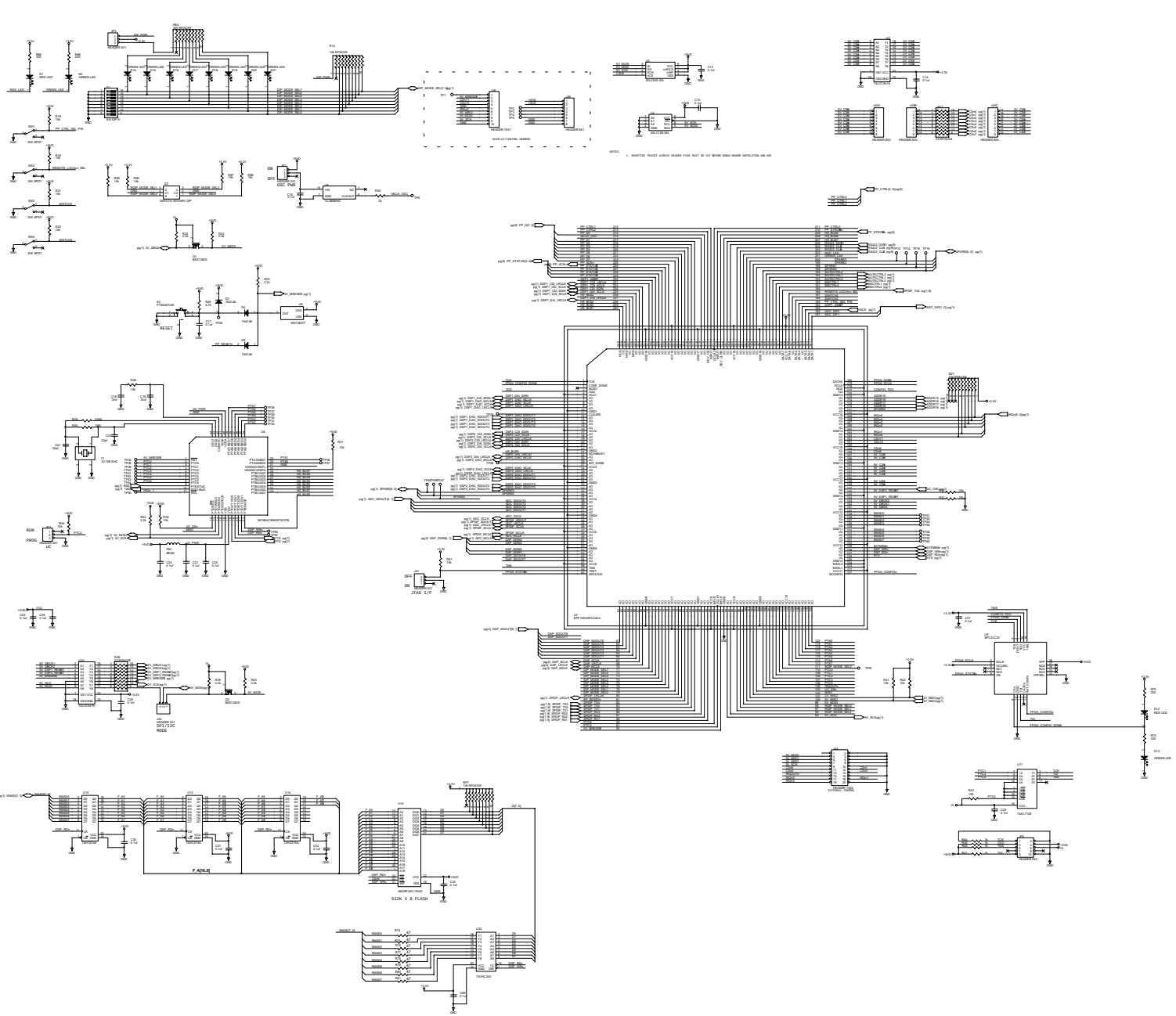


Figure 19. Sheet 4 - Microcontroller

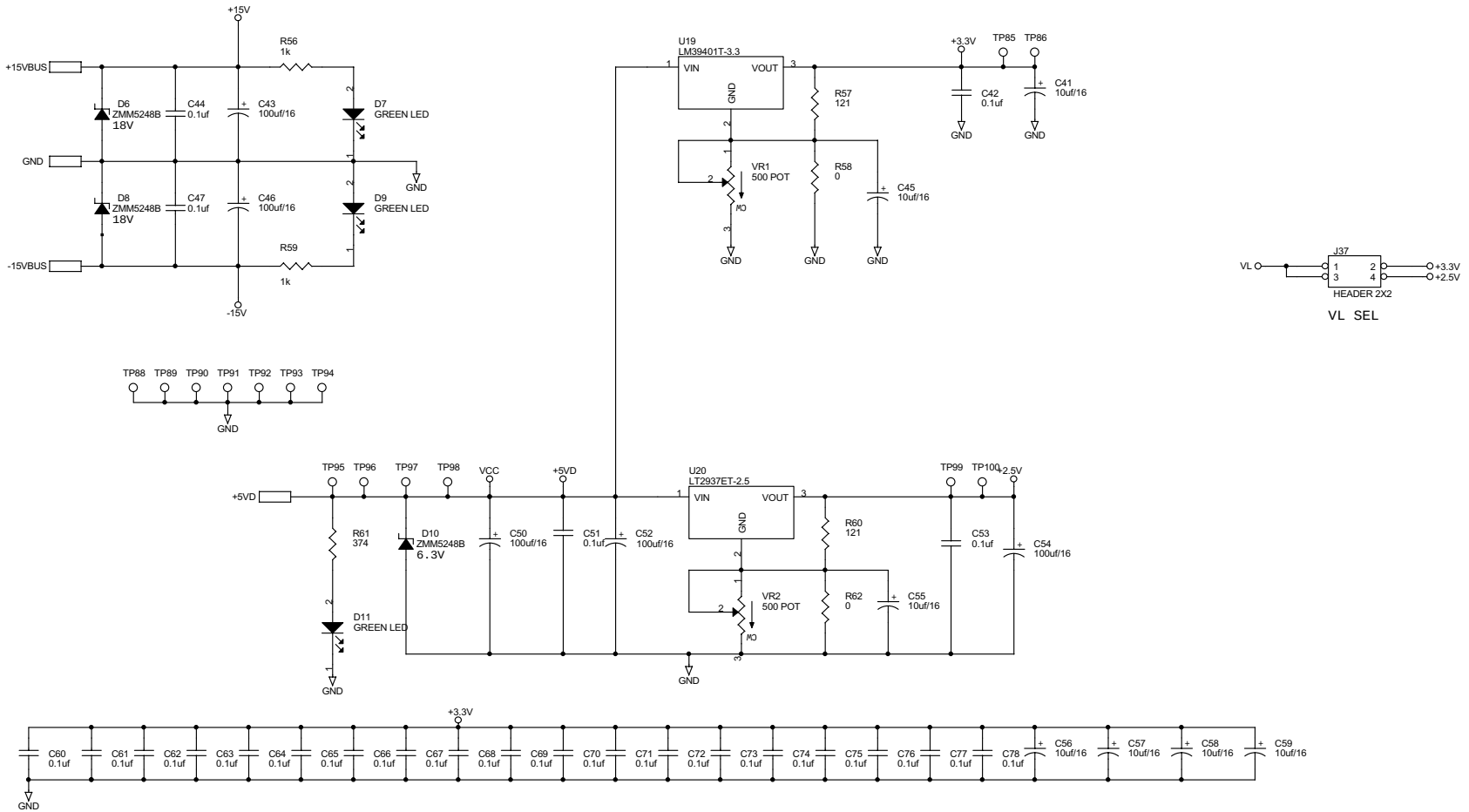


Figure 20. Sheet 5 - Power

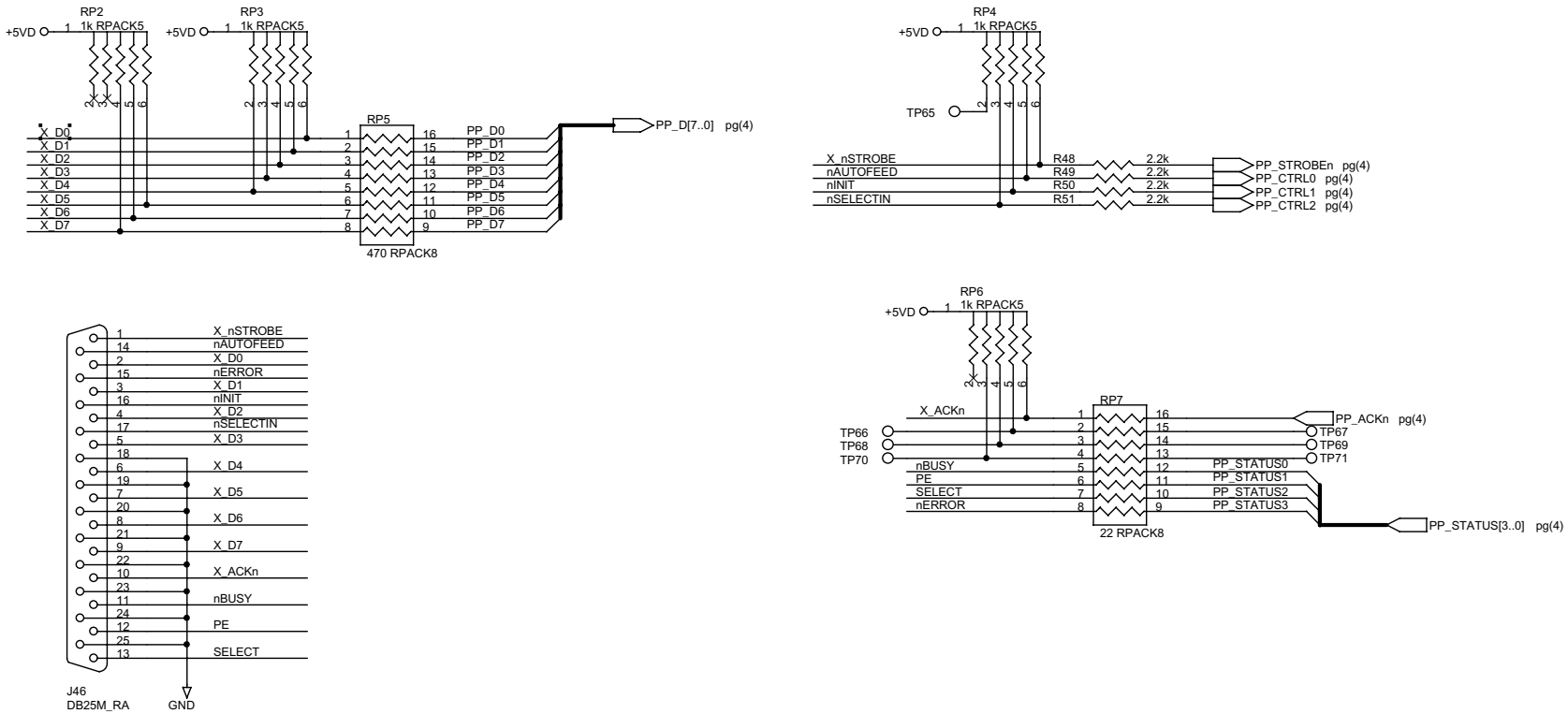


Figure 21. Sheet 6 - Parallel Port Interface

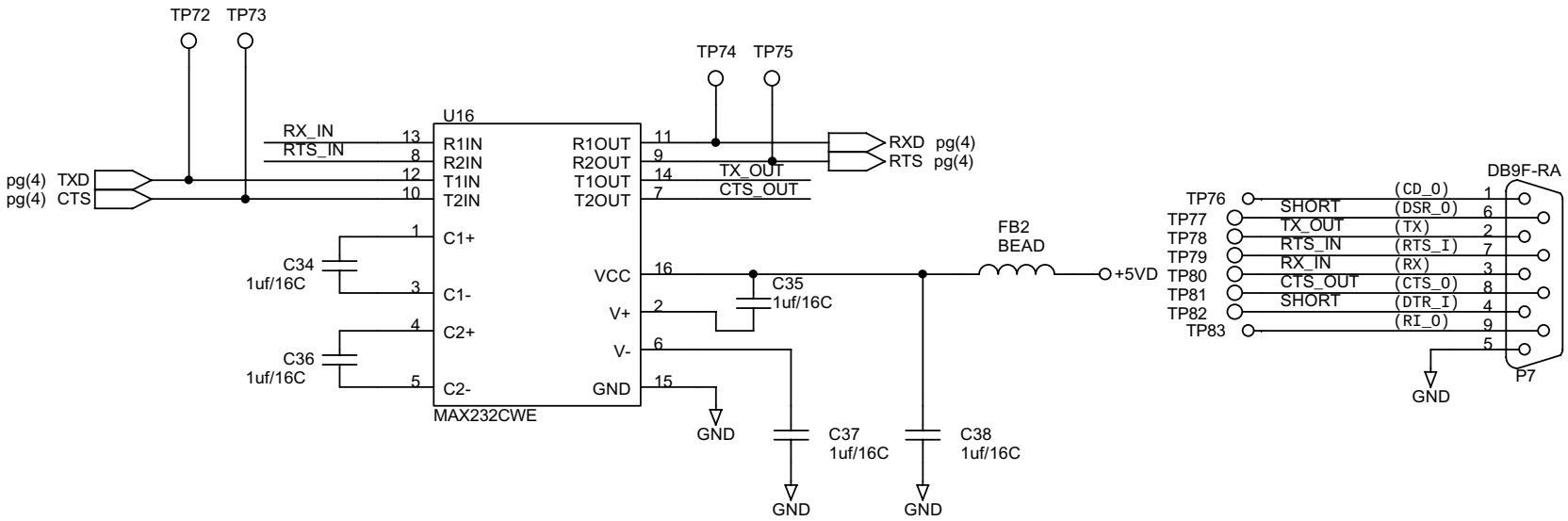


Figure 22. Sheet 7 - RS232 Interface

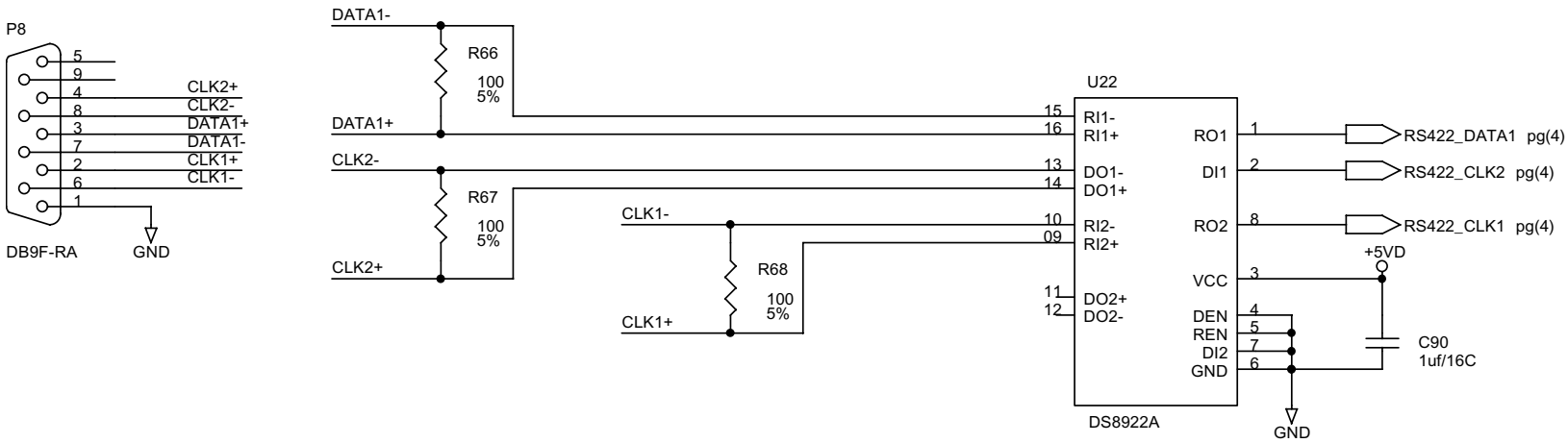


Figure 23. Sheet 8 - RS422 Interface

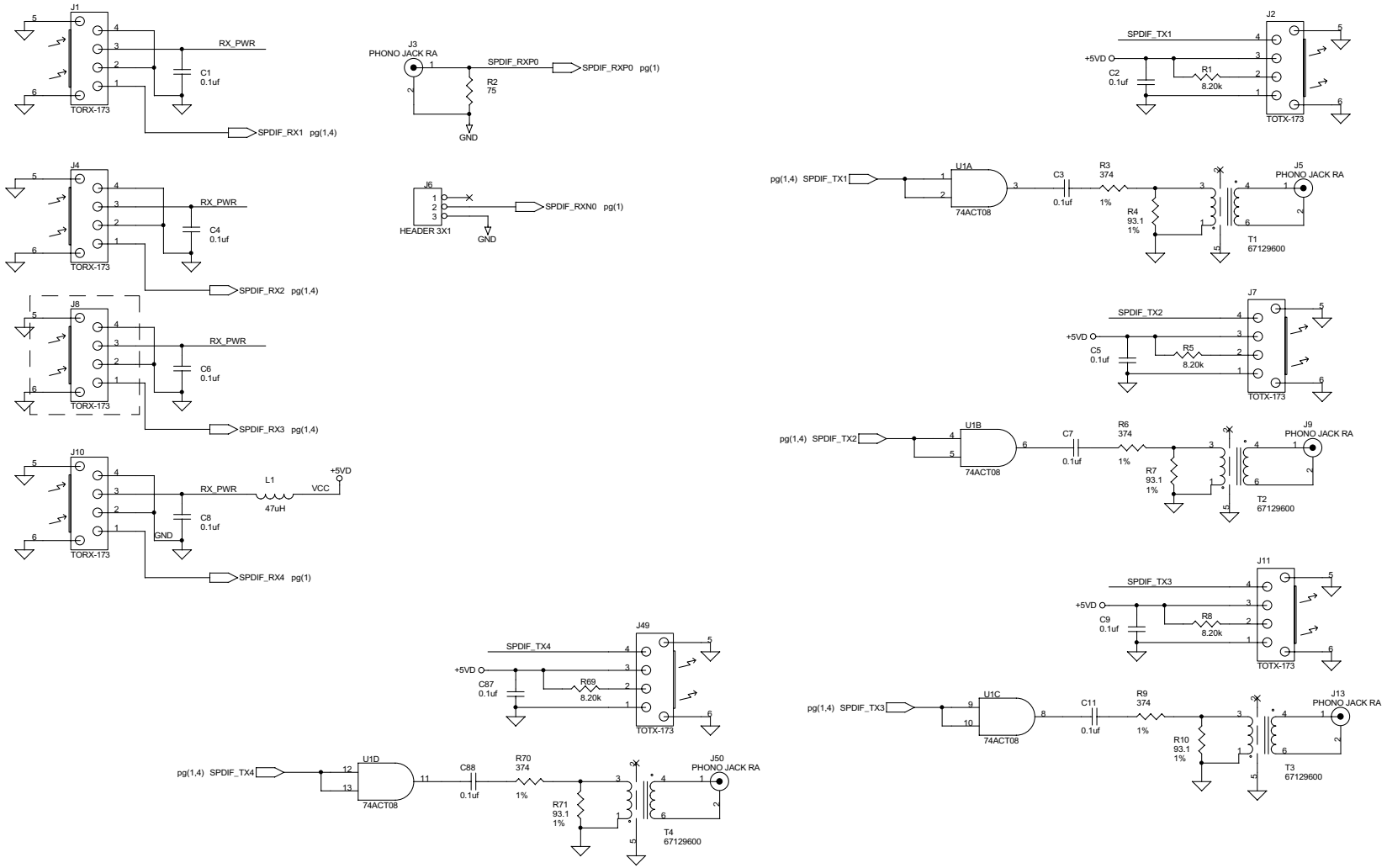


Figure 24. Sheet 9 - S/PDIF Receivers/Transmitters

APPENDIX J: BILL OF MATERIALS - UDSP

Item	Qty	Reference	MFG_PN	MFG	DESCRIPTION
1	57	C1 C2 C3 C4 C5 C6 C7 C8 C9 C11 C13 C14 C15 C16 C17 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C39 C40 C42 C44 C47 C51 C53 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C83 C87 C88 C89	C1206C104K5RAC	KEMET	CAP CERAMIC 0.1UF 50V 10% X7R 1206
2	1	C18	C1206C103K1RAC	KEMET	CAP CERAMIC 10NF 100V 10% X7R 1206
3	1	C19	C1206C333K1RAC	KEMET	CAP CERAMIC 33NF 100V 10% X7R 1206
4	2	C21 C20	C1206C220J1GAC	KEMET	CAP CERAMIC 22PF 100V 5% COG 1206
5	6	C34 C35 C36 C37 C38 C90	C1206C105M4RAC	KEMET	CAP CERAMIC 1UF 16V 20% 1206
6	5	C41 C56 C57 C58 C59	ECE-V1CA100SR	PANASONIC	CAP ELECT AL 10UF 16V 20% SM_B
7	7	C43 C46 C50 C52 C54 C80 C82	ECE-V1CA101WP	PANASONIC	CAP ELECT AL 100UF 16V 20% SM_D
8	2	C55 C45	ECE-V1CA100SR	PANASONIC	CAP ELECT AL 10UF 16V 20% SM_B
9	3	C79 C81 C84	ECE-V1HS010SR	PANASONIC	CAP 1uF ELEC VS SERIES SMT CASE-A 50V 20%
10	2	D1 D12	LN1251C-(TR)	PANASONIC	LED RED DIFF 10MA SM
11	13	D2 D7 D9 D11 D13 D14 D15 D16 D17 D18 D19 D20 D21	LN1351C-(TR)	PANASONIC	LED GREEN DIFF 10MA SM
12	3	D3 D4 D5	LL4148DI	VISHAY	DIODE HS SWITCHING MELF SOD-80
13	3	D6 D8 D10	ZMM5248B	VISHAY	DIODE ZENER 18V 500MW SOD-80
14	2	FB1 FB2	EXC-ML45A910U	PANASONIC	FERRITE BEAD 1806
15	6	JP1 JP2 JP5 J6 J41 J44	TSW-103-07-G-S	SAMTEC	HEADER MALE 0.1 IN HDR3X1
16	1	JP3	TSW-105-07-G-D	SAMTEC	HEADER MALE 0.1 IN HDR5X2
17	1	JP4	TSW-116-07-T-D	SAMTEC	STAKE HEADER 16X2 .1"" CENTER TIN
18	4	J1 J4 J8 J10	TORX-173	TOSHIBA	OPTICAL TOSLINK RECIEVER
19	4	J2 J7 J11 J49	TOTX-173	TOSHIBA	OPTICAL TRANSMITTER
20	21	J3 J5 J9 J13 J15 J16 J17 J18 J19 J20 J21 J22 J23 J24 J25 J26 J27 J29 J31 J33 J50	ARJ2018	A/D ELECT	PHONO JACK RA GOLD
21	1	J28	111-0110-001	E.F.JOHNSON	BINDING POST BLUE BPOST
22	1	J30	111-0103-001	E.F.JOHNSON	BINDING POST BLACK BPOST

Item	Qty	Reference	MFG_PN	MFG	DESCRIPTION
23	1	J32	111-0104-001	E.F.JOHNSON	BINDING POST GREEN BPOST
24	1	J34	111-0102-001	E.F.JOHNSON	BINDING POST RED BPOST
25	4	JX28 JX30 JX32 JX34	"1-1.5 X.25'TIN X.25"" TIN	TYPE E"	SQUIRES
26	1	J35	SDS-50J	CUI STACK	CONNECTOR CIRCULAR DIN5M
27	2	J36 J47	TSW-103-07-G-D	SAMTEC	HEADER MALE 0.1 IN HDR3X2
28	1	J37	TSW-102-07-G-D	SAMTEC	HEADER MALE 0.1 IN HDR2X2
29	1	J38	TSW-110-07-G-S	SAMTEC	HEADER MALE 0.1 IN HDR10X1
30	1	J39	TSW-108-07-G-S	SAMTEC	HEADER MALE 0.1 IN HDR8X1
31	1	J40	TSW-108-07-G-T	SAMTEC	HEADER MALE 0.1 IN HDR8X3
32	2	J45 J48	TSW-110-07-G-D	SAMTEC	HEADER MALE 0.1 IN HDR10X2
33	1	J46	747238-4	AMP	CONNECTOR DB25 MALE RA
34	1	J51	CON-AD3056-50	A/D ELECTRON-ICS	CONNECTOR STEREO HEADPHONE JACK
35	1	L1	ELJ-FA470KF	PANASONIC	INDUCTOR 47UH 1210
36	1	P1	ESQT-116-03-G-D-375	SAMTEC	HEADER FEMALE 2MM SOK16X2-2MM
37	4	P2 P3 P5 P6	ESQT-120-03-G-D-375	SAMTEC	HEADER FEMALE 2MM SOK20X2-2MM
38	1	P4	ESQT-107-03-G-D-375	SAMTEC	HEADER FEMALE 2MM SOK7X2-2MM
39	2	P8 P7	745781-4	AMP	CONNECTOR D-SHELL9 RA .318 MOUNT FEMALE
40	2	Q2 Q1	BSS138ZX	ZETEX	MOSFET N CH 1.5VT SOT23
41	3	RP1 R14 R27	4610X-101-103	BOURNS	RES R-PACK9 10K 1/8W 2% SIP10
42	2	RP2 RP3	4606X-101-102	BOURNS	RES R-PACK5 1K 1/8W 2% SIP6
43	2	RP4 RP6	4606X-101-102	BOURNS	RES R-PACK5 1K 1/8W 2% SIP6
44	1	RP5	4816P-T01-220	BOURNS	RES R-PACK8 221/8W 2% SO16N
45	4	RP7 RP8 R17 R38	4816P-T01-220	BOURNS	RES R-PACK8 22 1/8W 2% SO16N
46	4	R1 R5 R8 R69	ERJ-8GEYJ822	PANASONIC	RES THICK FILM 8.20K 1/8W 5% 1206
47	1	R2	ERJ-8ENF75R0	PANASONIC	RES THICK FILM 75 1/8W 5% 1206
48	5	R3 R6 R9 R61 R70	ERJ-8ENF3740	PANASONIC	RES THICK FILM 374 1/8W 1% 1206
49	4	R4 R7 R10 R71	ERJ-8ENF93R1	PANASONIC	RES THICK FILM 93.1 1/8W 1% 1206
50	5	R11 R12 R13 R26 R65	ERJ-8GEYJ472	PANASONIC	RES THICK FILM 4.7K 1/8W 5% 1206

Item	Qty	Reference	MFG_PN	MFG	DESCRIPTION
51	20	R18 R19 R21 R22 R28 R31 R32 R33 R35 R36 R37 R41 R42 R43 R82 R83 R87 R88 R89 R90	ERJ-8ENF1002	PANASONIC	RES THICK FILM 10K 1/8W 1% 1206
52	5	R20 R52 R53 R54 R55	ERJ-8GEYJ330	PANASONIC	RES THICK FILM 33 1/8W 5% 1206
53	10	R23 R24 R25 R34 R39 R40 R48 R49 R50 R51	ERJ-8GEYJ222	PANASONIC	RES THICK FILM 2.2K 1/8W 5% 1206
54	1	R29	ERJ-8GEYJ334	PANASONIC	RES THICK FILM 330K 1/8W 5% 1206
55	1	R30	ERJ-8GEYJ106	PANASONIC	RES THICK FILM 10MEG 1/8W 5% 1206
56	6	R44 R45 R46 R47 R56 R59	ERJ-8GEYJ102	PANASONIC	RES THICK FILM 1K 1/8W 5% 1206
57	2	R60 R57	ERJ-8ENF1210	PANASONIC	RES THICK FILM 121 1/8W 1% 1206
58	2	R62 R58	ERJ-8GEY0R00V	PANASONIC	RES THICK FILM 0 1/8W 5% 1206
59	3	R66 R67 R68	CRCW12061000F	DALE	RES 100 OHMS 1206 1/8W 1% 100ppm
60	4	R72 R73 R85 R86	ERJ-8GEYJ331	PANASONIC	RES THICK FILM330 1/8W 5% 1206
61	8	R74 R75 R76 R77 R78 R79 R80 R81	ERJ-8GEYJ470V	PANASONIC	RES 49.9-OHM 1% 0805 1/10W
62	1	R84	4610X-101-331	BOURNS	RES R-PACK9 330 1/8W 2% SIP10
63	4	SW1 SW2 SW3 SW4	TS01CBE	C&K	SWITCH SLIDE SPDT
64	1	S1	76SB08	GRAYHILL	SWITCH DIP 8 POS ROCKER DIP16
65	1	S2	94HBB16	GRAYHILL	SWITCH DIP ROTARY HEX SM
66	1	S3	PTS645TL50	C&K	SWITCH 6MM TACT W/ ESD PIN 130GF DPST
67	78	TP1 TP2 TP3 TP4 TP5 TP6 TP13 TP14 TP15 TP16 TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP34 TP35 TP36 TP37 TP38 TP39 TP40 TP41 TP42 TP43 TP44 TP45 TP46 TP47 TP50 TP51 TP52 TP53 TP54 TP55 TP56 TP57 TP58 TP59 TP60 TP61 TP65 TP66 TP67 TP68 TP69 TP70 TP71 TP72 T	NONE	NONE	TEST POINT PAD62H40
68	4	T1 T2 T3 T4	67129600	SCHOTT	TRANSFORMER TH
69	1	U1	74ACT08SC	FAIRCHILD	IC QUAD AND GATE SO14N
70	2	U2 U10	SN74LVC541ADW	TI	IC OCTAL BUFFER SO20-300
71	1	U3	25LC640I-SN	MICROCHIP	IC EEPROM SERIAL SPI 8KX8 SO8N
72	1	U4	24LC128I-SN	MICROCHIP	IC EEPROM I2C SERIAL 16KX8 SO8N

Item	Qty	Reference	MFG_PN	MFG	DESCRIPTION
73	1	U5	CX21AF-12.2880MHZ	CAL CRYSTAL	IC OSCILLATOR 12.2880MHZ 50PPM OSC14
74	4	UX5	8134-HC-5P2	AUGAT	S0CKET PIN P0P-INSM
75	1	U6	MN13821T	PANASONIC	IC VOLTAGE DETECTOR OD 4.4-4.7V SC59A
76	1	U7	EPF10K30AQC240-1	ALTERA	IC FPGA -4 PQFP240
77	1	U8	MC68HC908GP32CFB	MOTOROLA	IC MICROCONTROLLER 32K PQFP44
78	1	U9	EPC2LC20	ALTERA	IC CONFIG EEPROM PLCC20
79	1	UX9	540-99-020-17-40000	MILL-MAX	S0CKET PLCC-20 SMT
80	2	U11 U18	MM74ACT125AD	FAIRCHILD	IC QUAD BUFFER W/ 3-STATE SO14-150
81	3	U12 U13 U14	SN74HCT574DW	TI	IC D-FLOP TRI-STATE OCTAL SO20-300
82	1	U15	AM29F040B-150JC	AMD	IC FLASH 512KX8 150NS 32PLCC
83	1	U16	MAX232CWE	MAXIM	IC RS232 TRANSCEIVER SO16W
84	1	U17	MM74ACT541AD	FAIRCHILD	IC BUFFER OCTAL SO20-300
85	1	U19	LM39401T-3.3	NATIONAL SEMI	IC VREG POSITIVE 3.3V TO220AB
86	1	U20	LT2937ET-2.5	LINEAR TECH	IC VREG POSITIVE 2.5V TO220AB
87	1	U21	LM4811MM	NATIONAL SEMI	IC HEADPHONE AMPLIFIER MSOP-8
88	1	U22	DS8922M	NATIONAL SEMI	IC RS422 DIFFERENTIAL LINE DRIVER SO16-240
89	1	U23	TC74VHC245FT	TOSHIBA	BI-DIR OCTAL BUFFER TRI-STATE TSSOP20
90	1	U24	EVQ-VEMF0224B	PANASONIC	ENCODER ROTARY
91	2	VR2 VR1	3296Y-501	BOURNS	RES POTENTIOMETER 500 25 TURN TOP ADJ TH
92	1	Y1	CM200S32.768KDZFT	CITIZEN	CRYSTAL 32.768 KHZ PARALLEL 12.5PF LOAD
93	8		313-6477-032	E.F. JOHNSON	STAND-0FF .875"" HT 1/4 FLAT 4-40 THREAD
94	8		H343-ND	DIGI-KEY	SCREW 4-40 5/16 MACHINE
95	1		UDSP-1B.0		PRINTED CIRCUIT BOARD


CIRRUS LOGIC®