

Errata: CS5378 Rev B Errata

(Reference the CS5378 data sheet revision DS639F2 dated SEP'08.)

Erratum #1: $\overline{\text{DRDY}}$ Lock Condition

Description

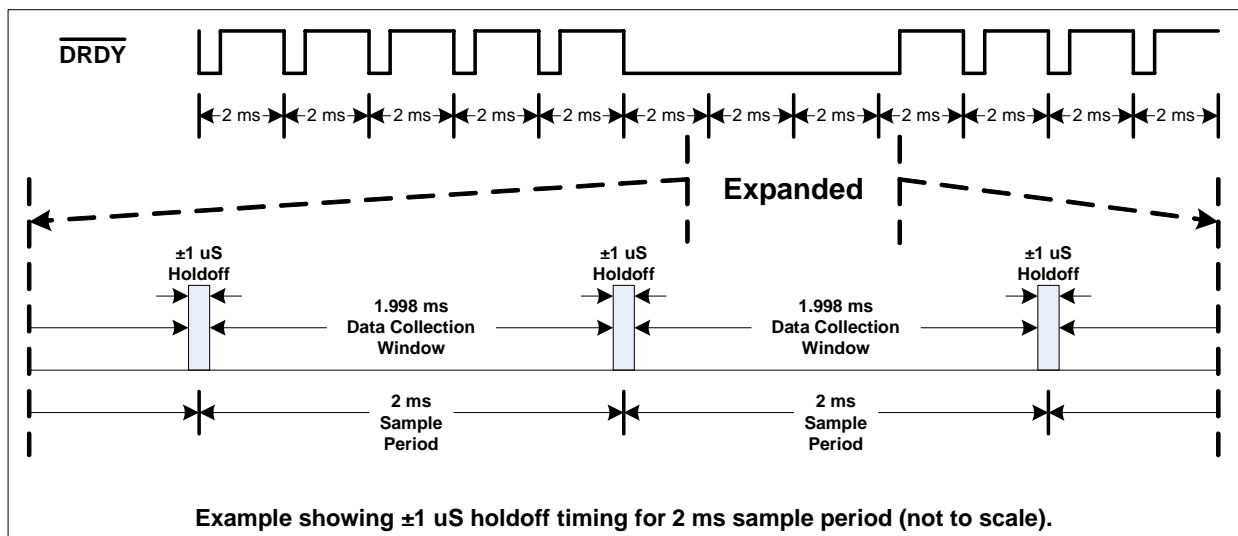
When the CS5378 revB device has data available in the output FIFO it asserts the $\overline{\text{DRDY}}$ pin low to signal the external system to initiate a data collection transaction.

If the external data collection transaction is initiated coincident with a subsequent data word being written into the output FIFO the $\overline{\text{DRDY}}$ signal can permanently lock into a high or low state and no further data transactions can occur.

Workaround

This erratum is hardware related and requires a hardware reset if it occurs. This behavior can be prevented by always collecting data within one sample period after $\overline{\text{DRDY}}$ goes low so the output FIFO never contains more than one sample.

If the output FIFO must be used due to latency collecting data, carefully time the data collection transaction to avoid an integer sample period timing relative to the initial $\overline{\text{DRDY}}$ assertion. A holdoff of at least ± 1 μs is required around the integer sample period time.



Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find one nearest you go to www.cirrus.com

Erratum #2: Early Synchronization Timing

Description

Applying a rising edge to the CS5378 revB SYNC pin synchronizes the external analog sampling and internal digital filter state machine to a hardware generated MSYNC signal. The MSYNC signal timing is within 2 μ s of the incoming SYNC rising edge as shown in the timing diagram on page 16 of the data sheet.

Depending on the specific timing of the SYNC input relative to previous SYNC inputs (or the initialization 'Filter Start' command if SYNC has not been previously applied), it is possible for the digital filter state machine to synchronize 1/8 of a sample period earlier than expected. As an example, for 2 ms sampling, it is possible for the digital filter synchronization to be 250 μ s earlier than expected depending when the SYNC input is received relative to the previous SYNC input.

Workaround

Because this early synchronization condition only occurs when the SYNC input is received with a specific timing relative to a previous SYNC signal, a 'double-tap' SYNC input will guarantee proper synchronization. The external system should apply the first (asynchronous) SYNC input immediately and then delay exactly one or more integer sample periods and apply a second (synchronous) SYNC input.

Most CS5378 devices in a system receiving an asynchronous SYNC signal will not exhibit this early 1/8 sample period synchronization, so a second synchronous SYNC input will be transparent to normal operation. For the small number of devices in the system that do exhibit this early 1/8 sample period synchronization, the second synchronous SYNC input will correct the timing.

